
Basics of Jitter in Wireline Communications

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Outline

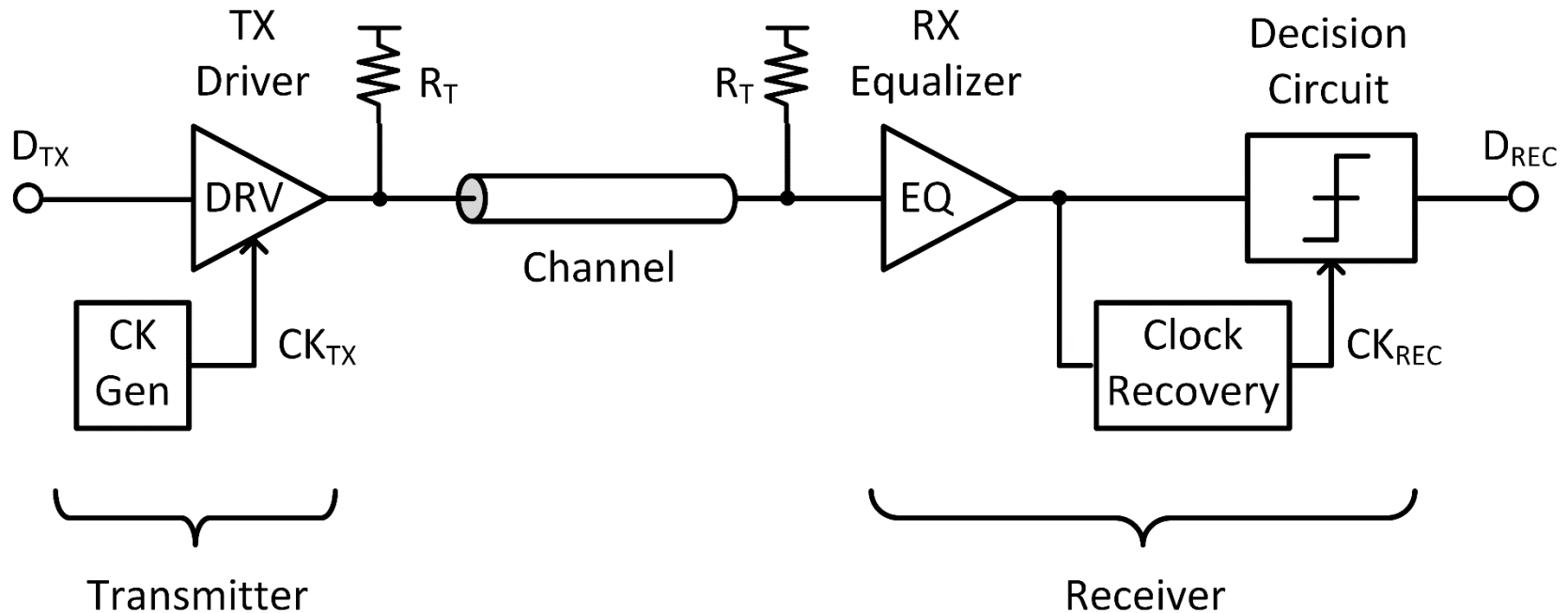
Part One: Basics of Jitter

- ☐ Motivation
- ☐ Jitter Definitions: What is Jitter?
- ☐ Characterizing and Classifying Jitter
- ☐ Example: Jitter in Ring Oscillator
- ☐ Summary of Part One

Part Two: Jitter in CDR

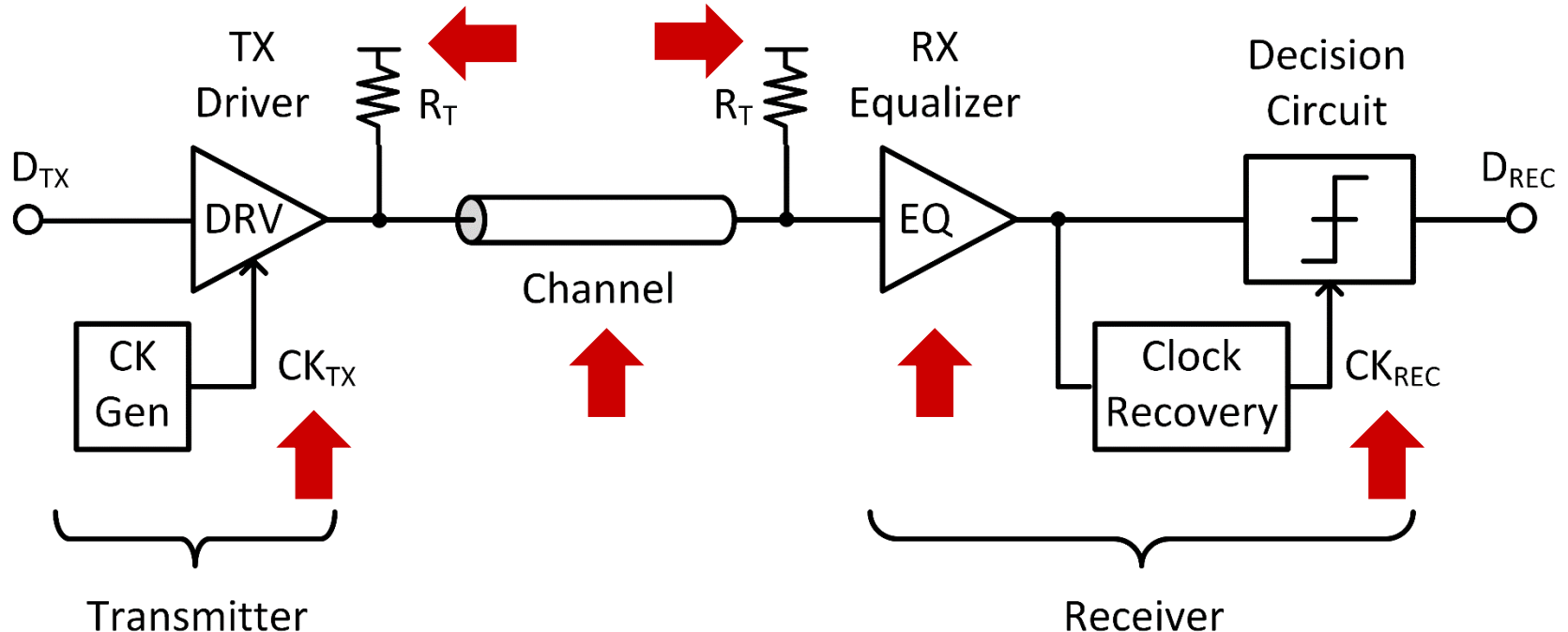
- ☐ Jitter in Clock and Data Recovery
- ☐ Effects of Jitter on Bang-Bang CDR Operation
- ☐ Jitter Monitoring and Jitter Mitigation
- ☐ Intentional Jitter: How Jitter can help
- ☐ Summary
- ☐ References

Wireline Transceiver Building Blocks



- ❑ Transceiver = Transmitter (TX) + Receiver (RX)
- ❑ TX pre-equalizes and sends data timed with CK_{TX}
- ❑ RX equalizes RX data, recovers CK_{REC} , and detects data
- ❑ Goal: Minimize Bit Error Rate (BER), typically $< 10^{-15}$

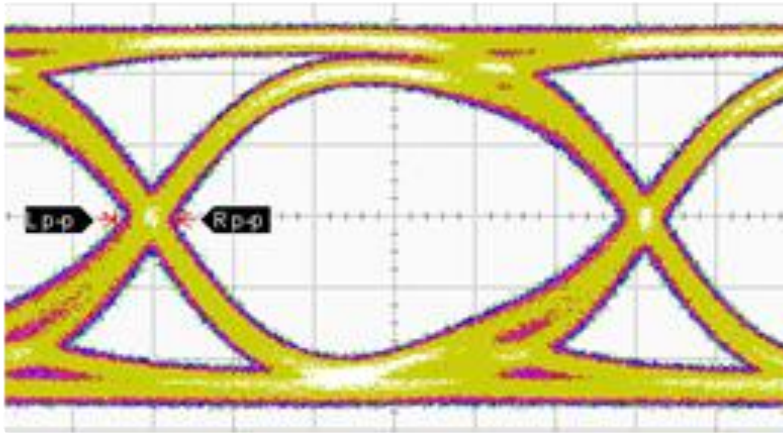
Effects of Timing Uncertainty on BER



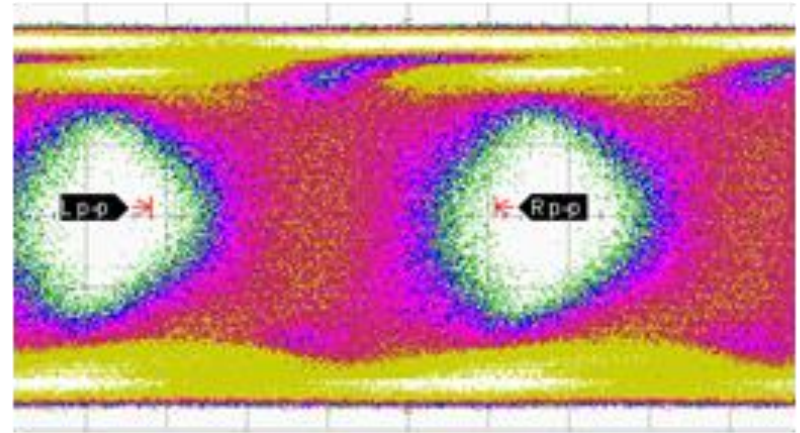
- ❑ No clock is perfect: they are either slow or fast
- ❑ Uncertainty as to when they are slow or fast
- ❑ VDD noise, channel, EQ, cross-talk contribute to this
- ❑ Timing uncertainty leads to errors in detected bits

Data Eye (with and without Jitter)

Without Jitter



With Jitter



- Data eye at decision point; almost closed w/ jitter
- Unacceptable bit error rate (BER) with jitter

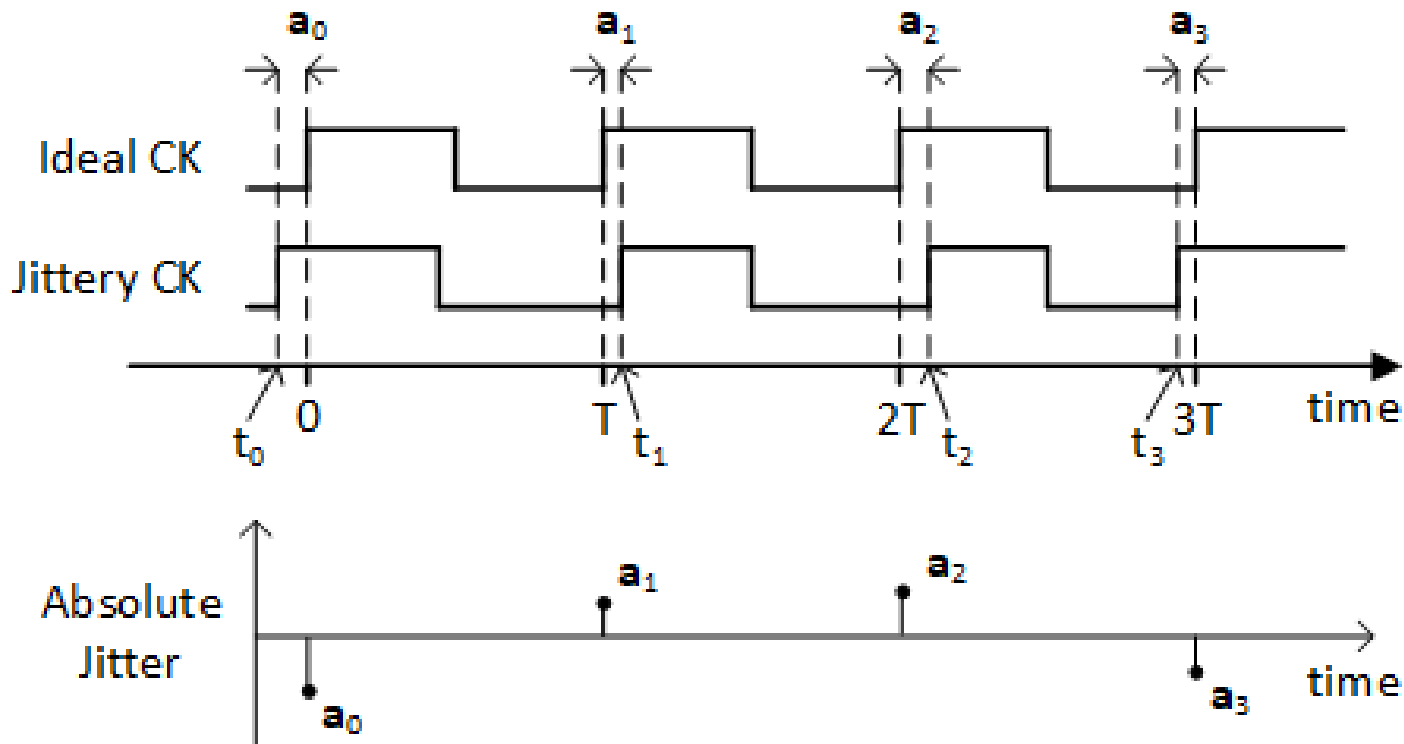
Three Questions:

1. Can we live with this timing uncertainty yet be precise?
2. How to monitor this and to reduce/mitigate it?
3. If jitter is enemy of BER, how to best defeat it?

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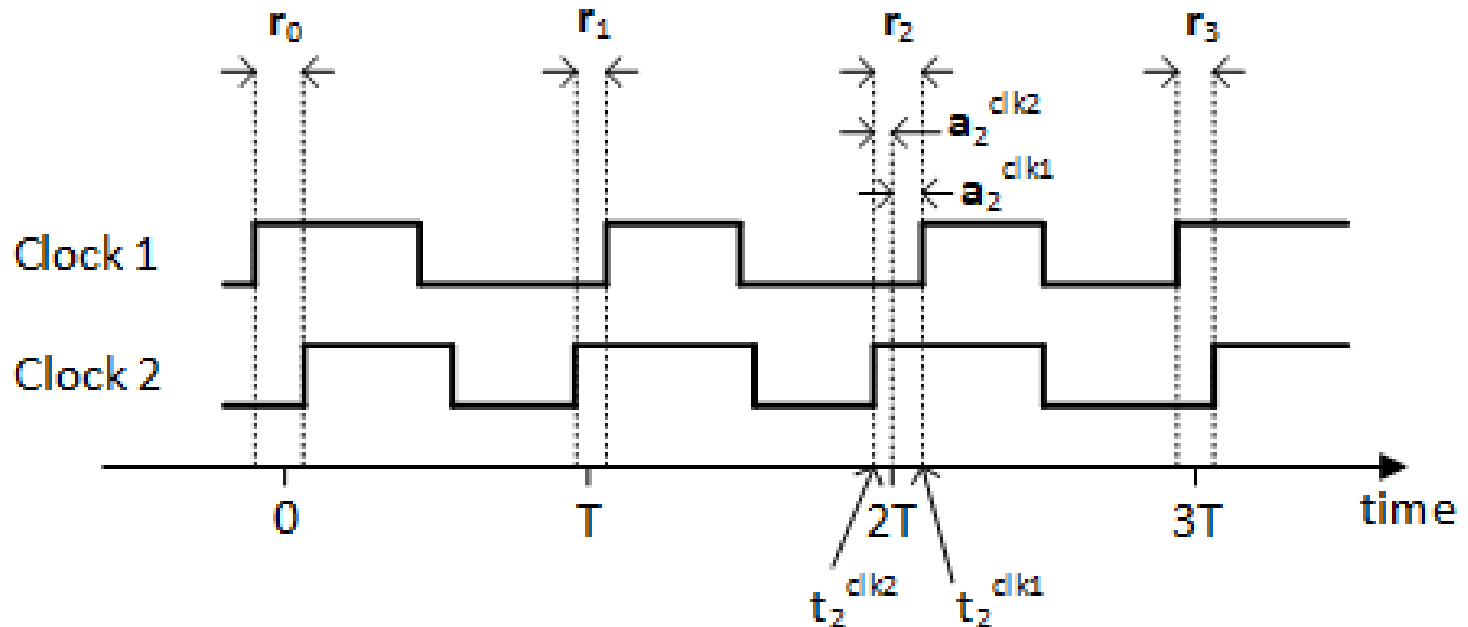
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Absolute Jitter



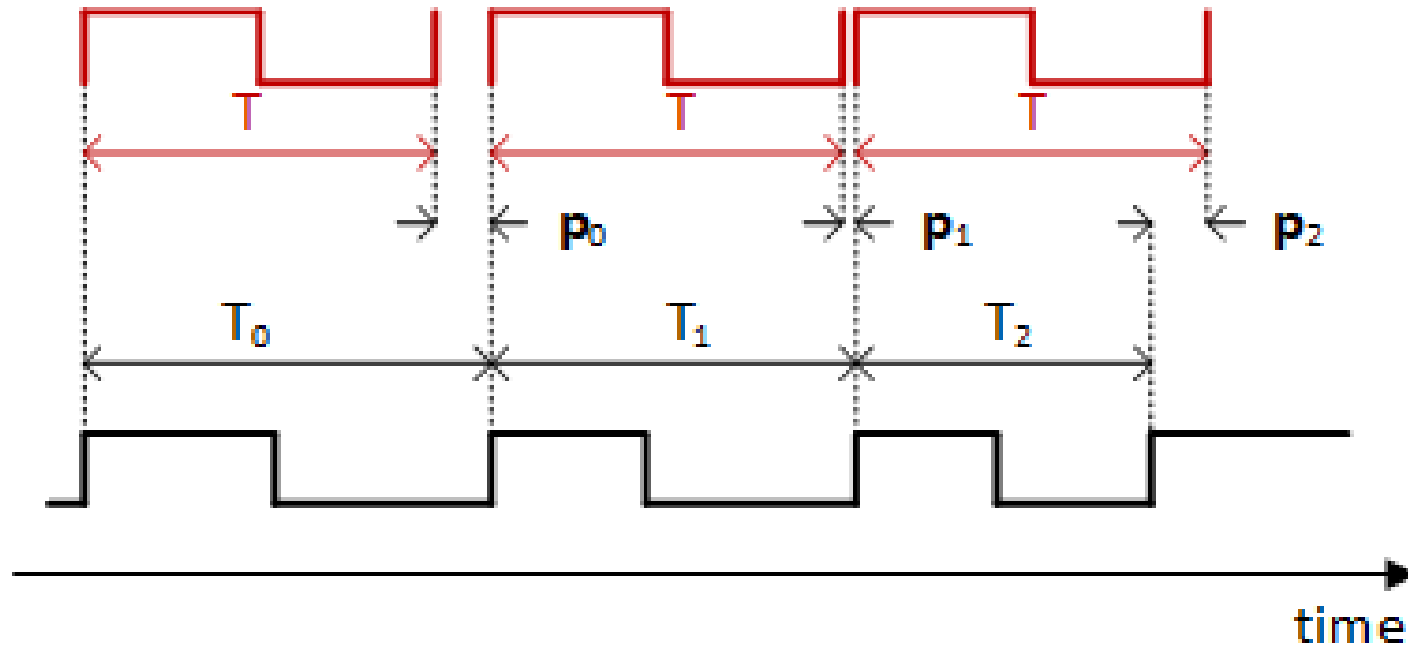
- Timing deviation between a jittery CK and an idea CK
- A discrete-time random signal, defined as $\mathbf{a}_k := t_k - kT$
- Never have an ideal clock; how is this useful?

Relative Jitter



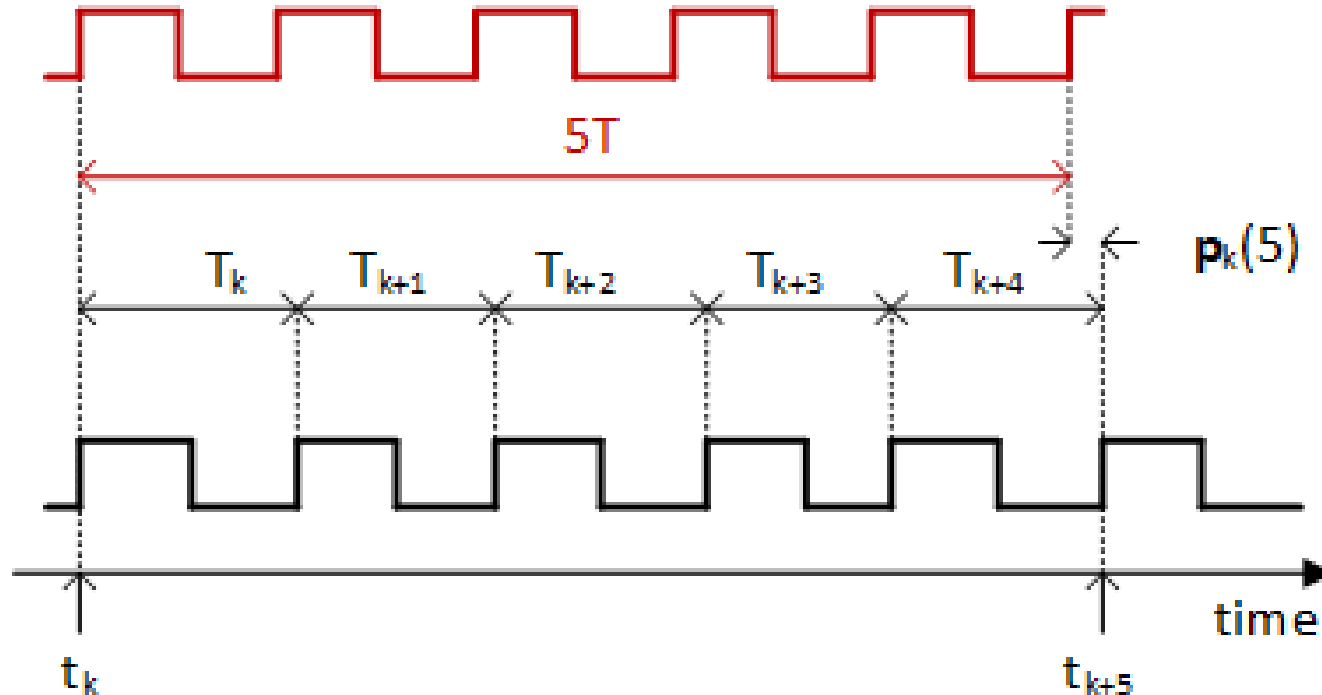
- Timing difference between two non-ideal clocks
- Another discrete-time random signal
- $\mathbf{r}_k := t_k(CK1) - t_k(CK2) = \mathbf{a}_k(CK1) - \mathbf{a}_k(CK2)$
- Where do we use this?

Period Jitter



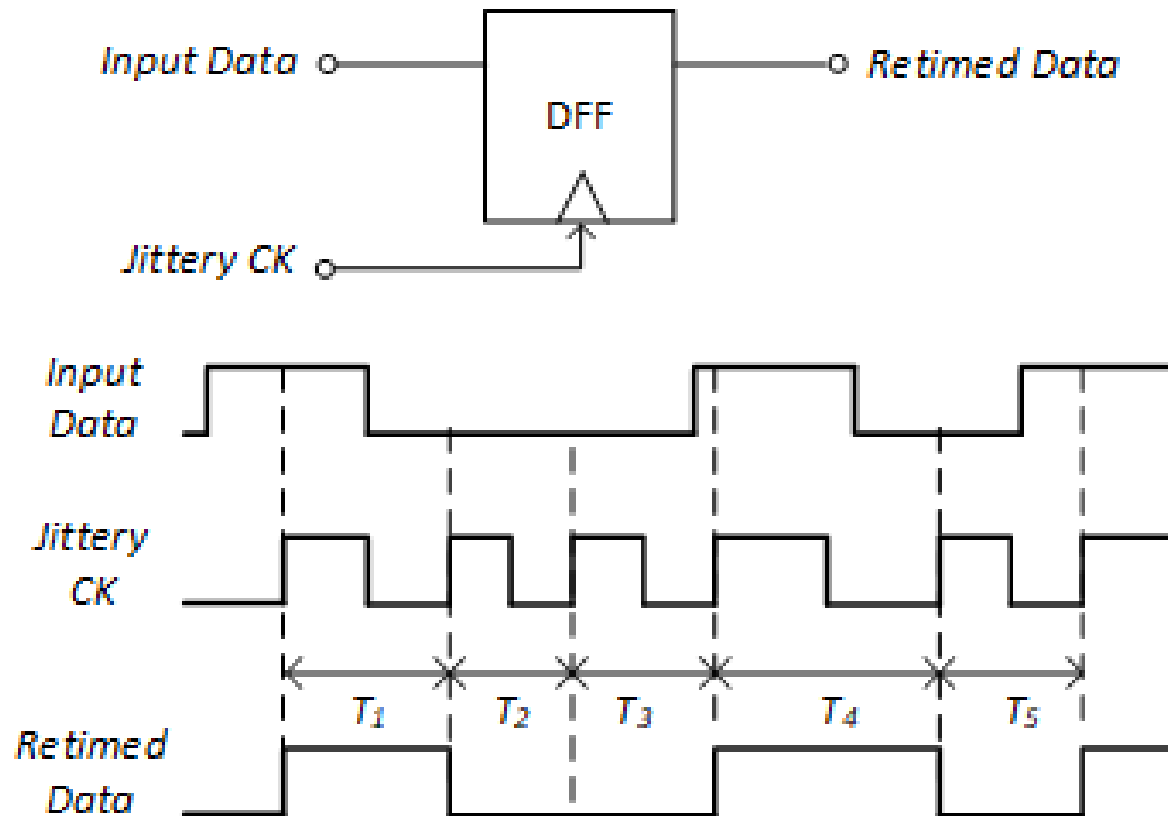
- Also known as Cycle Jitter, defined as the difference between edge-to-edge interval ("period") and the nominal period
- $p_k := (t_{k+1} - t_k) - T = T_k - T = a_{k+1} - a_k$
- Period jitter can be derived easily from absolute jitter
- Where do we use this?

N-Period Jitter



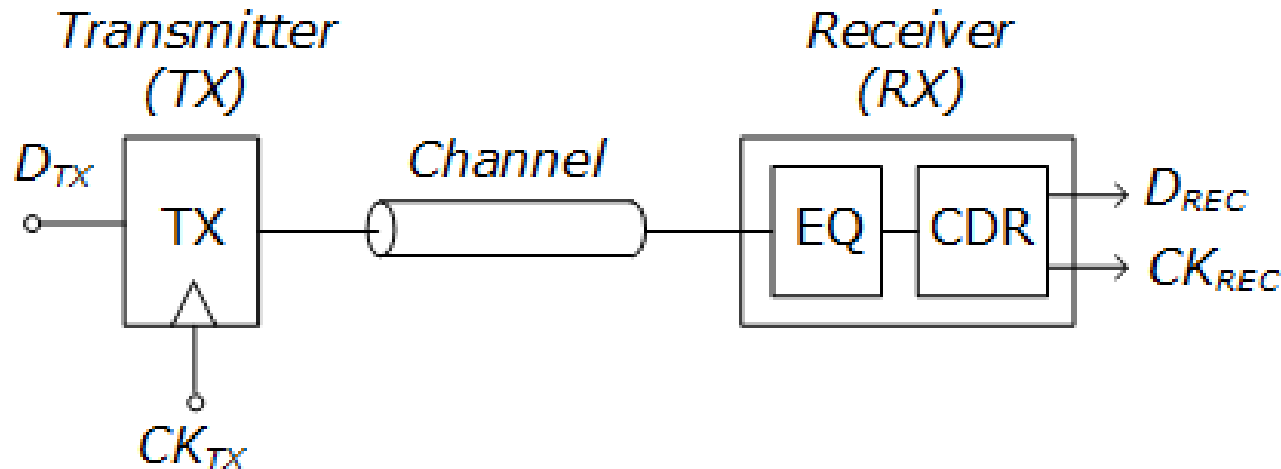
- Also known as Accumulation Jitter, defined as an accumulation of period jitter over N consecutive intervals
- $p_k(N) := (t_{k+N} - t_k) - NT = a_{k+N} - a_k$
- Where do we use this?

Data Jitter



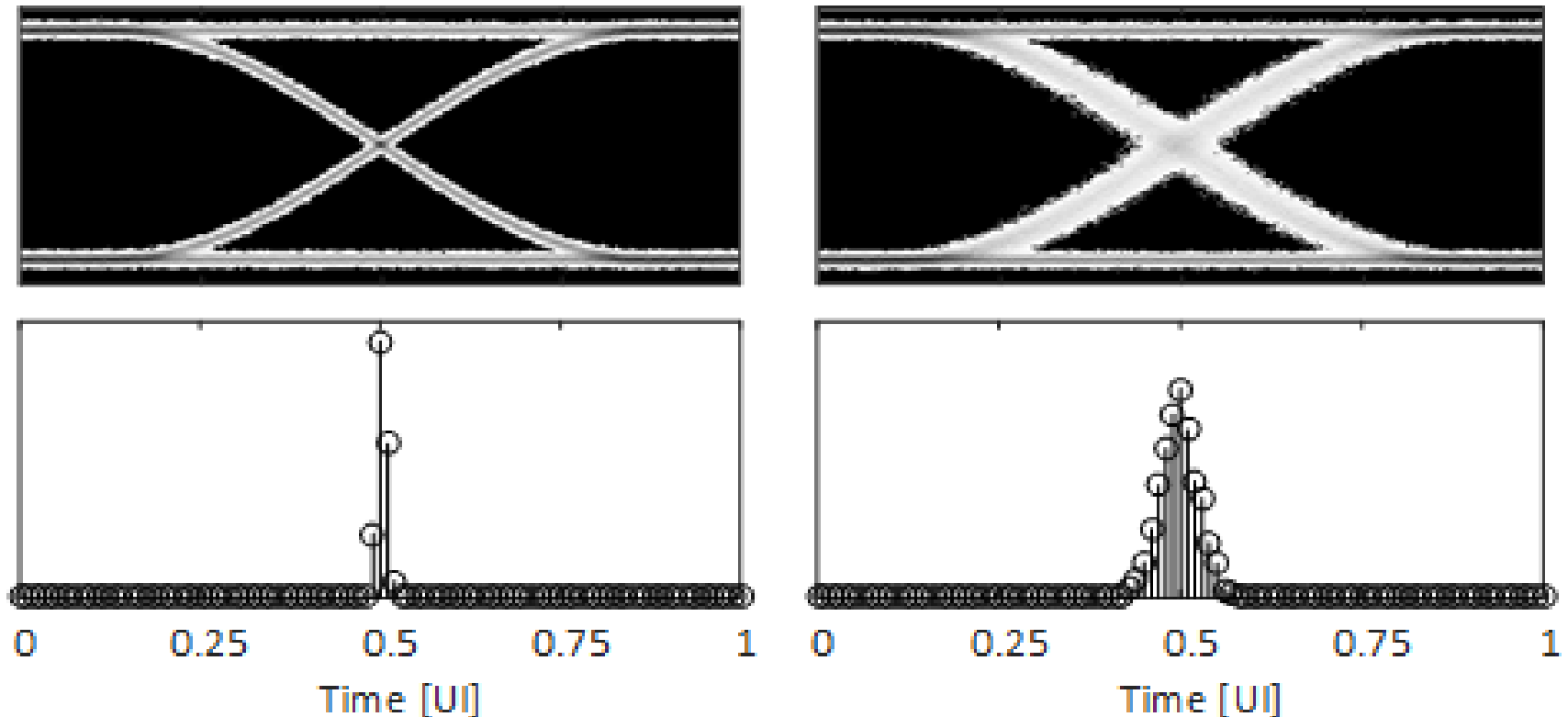
- ❑ Jittery CK retimes random binary input data
- ❑ Due to random nature of data sequence (i.e. lack of transitions), jitter not fully observable at the output

Data-Dependent Jitter



- ❑ Consider data at transmitter with no jitter
- ❑ Data is binary random sequence; random transition
- ❑ Channel has limited bandwidth; acts like RC
- ❑ A transition moves depending on preceding data
- ❑ This produces **Data-Dependent Jitter (DDJ)**
- ❑ Type of **Deterministic Jitter (DJ)** because it is predictable
- ❑ In contrast with **Random Jitter (RJ)** we discussed

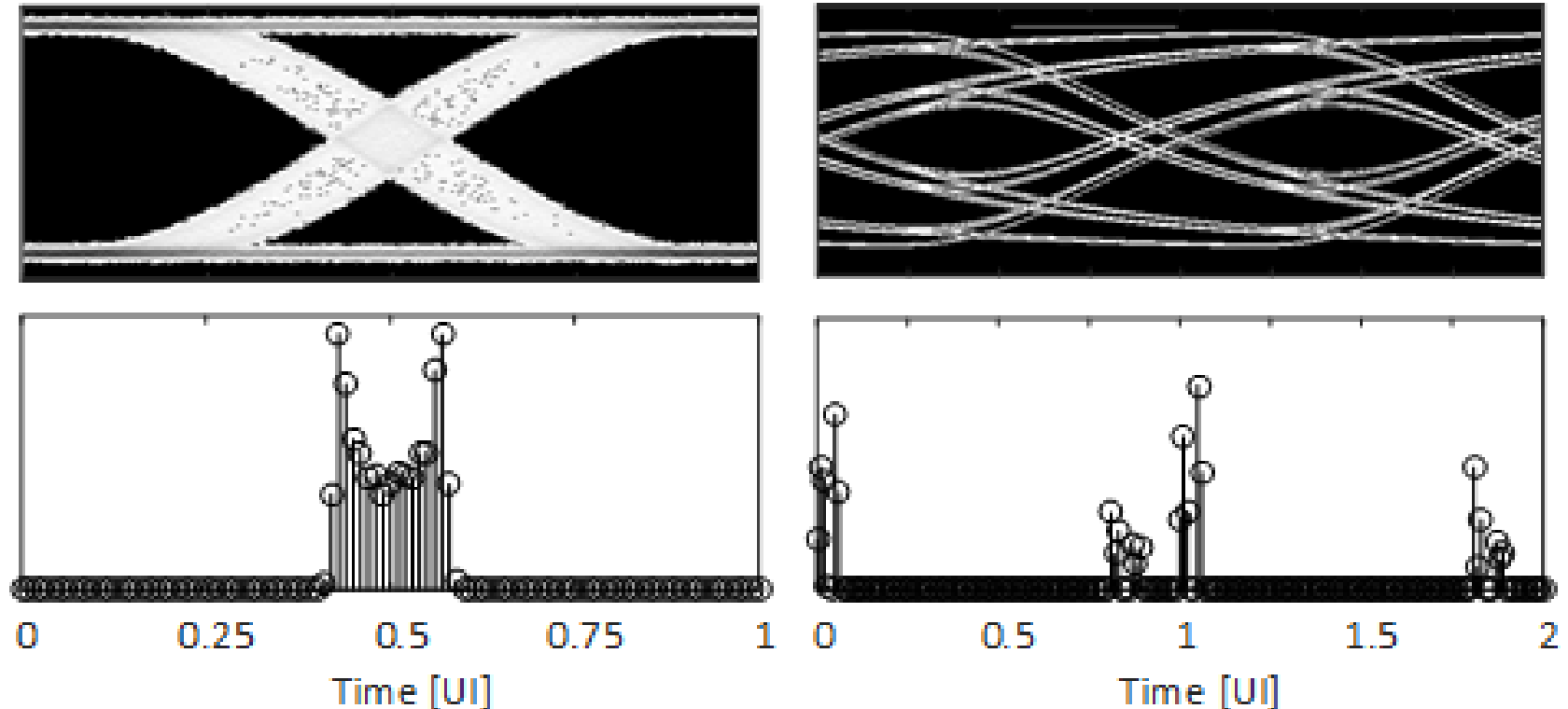
No Jitter versus Random Jitter (RJ)



- ❑ One sharp transition
- ❑ Histogram like a delta

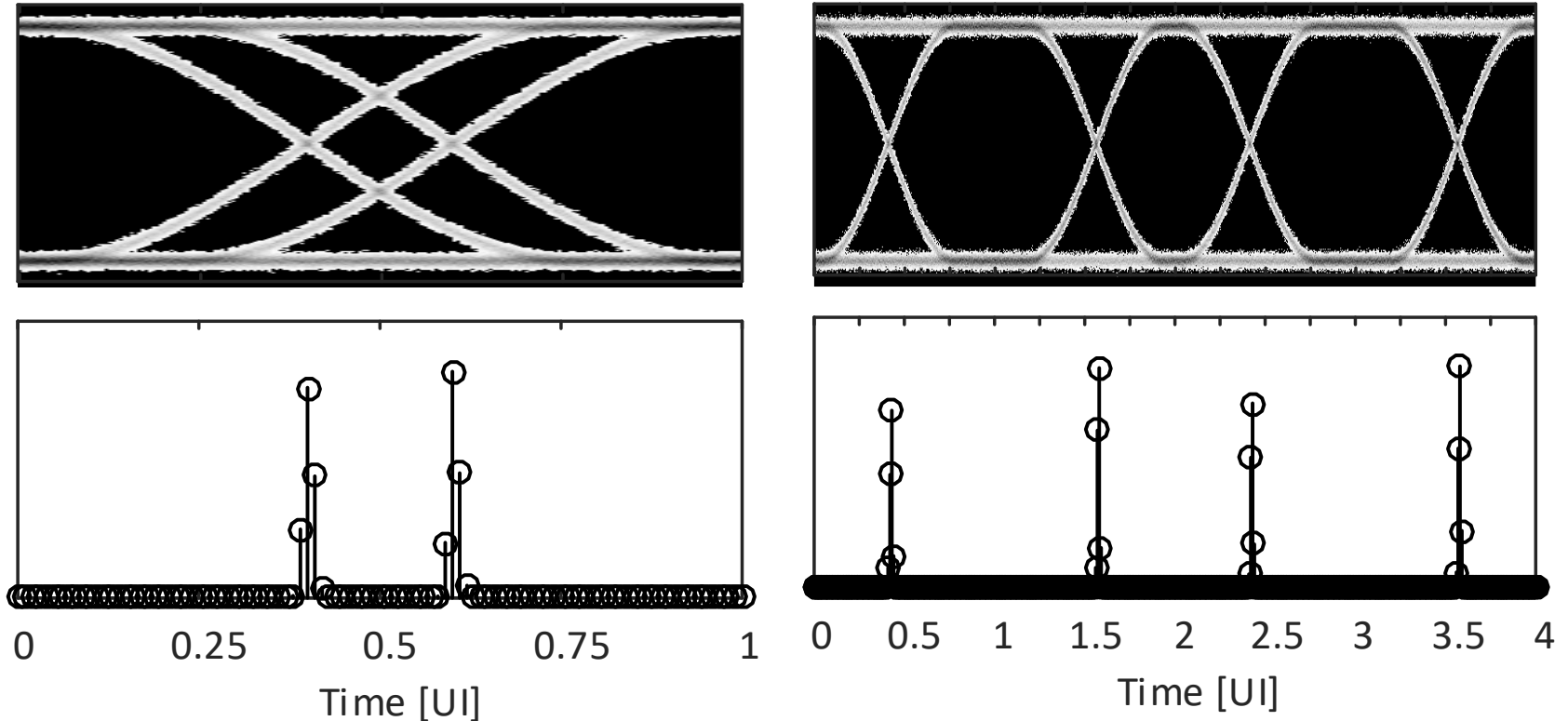
- ❑ Transitions distributed
- ❑ Gaussian Histogram
- ❑ Unbounded Jitter

Bounded/Deterministic Jitter



- ❑ Sinusoidal jitter
- ❑ Histogram of sine
- ❑ Used to characterize links
- ❑ Inter-Symbol Interference (ISI) induced jitter
- ❑ Deterministic, bounded

Duty-Cycle Distortion (DCD)



- DCD-Induced jitter
- Histogram over one UI
- UI: Unit Interval

- DCD-Induced jitter
- Histogram over 4 UIs

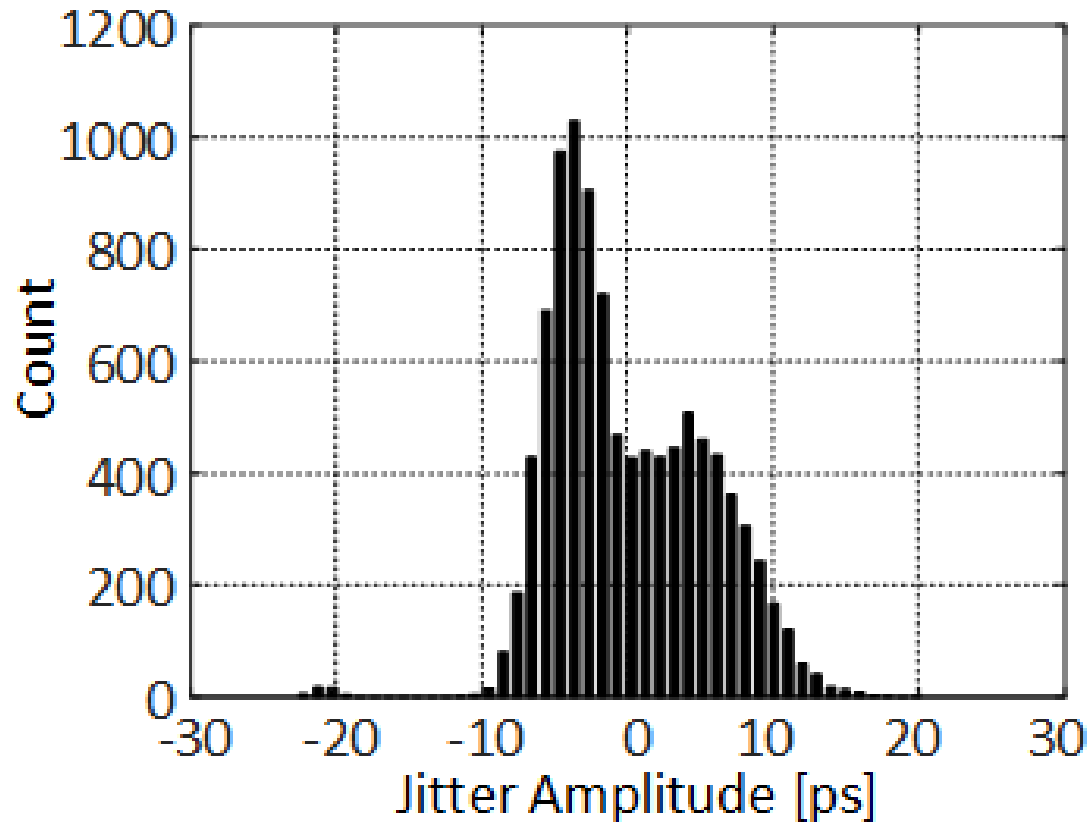
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Characterizing Jitter

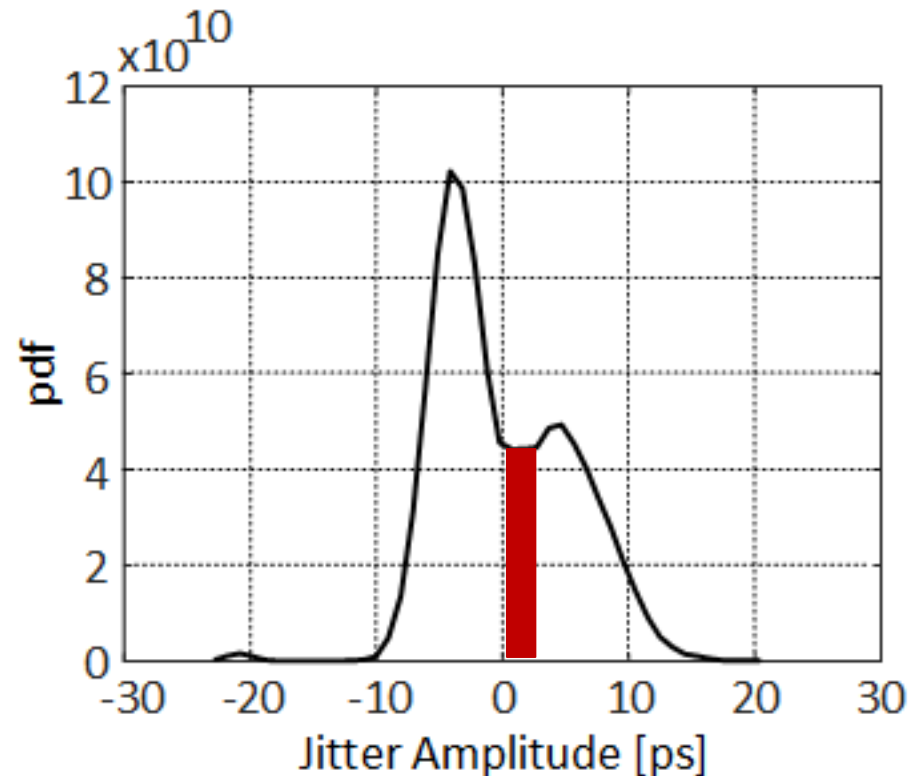
- What we said so far:
 - Jitter in all its forms (absolute, relative, period, N-period) is a discrete-time random signal
 - Interestingly, all can be derived from absolute jitter
 - Data jitter can be deterministic, data dependent
- How do we characterize a random signal?
- **Statistics:**
 - **Histogram**, Probability Density Function (PDF)
 - mean, rms, signal power
- **Time Domain:**
 - How the signal statistics changes with time
 - Autocorrelation function
- **Frequency Domain:**
 - Fourier of Autocorrelation function: Power Spectral Density (PSD)

Jitter Histogram



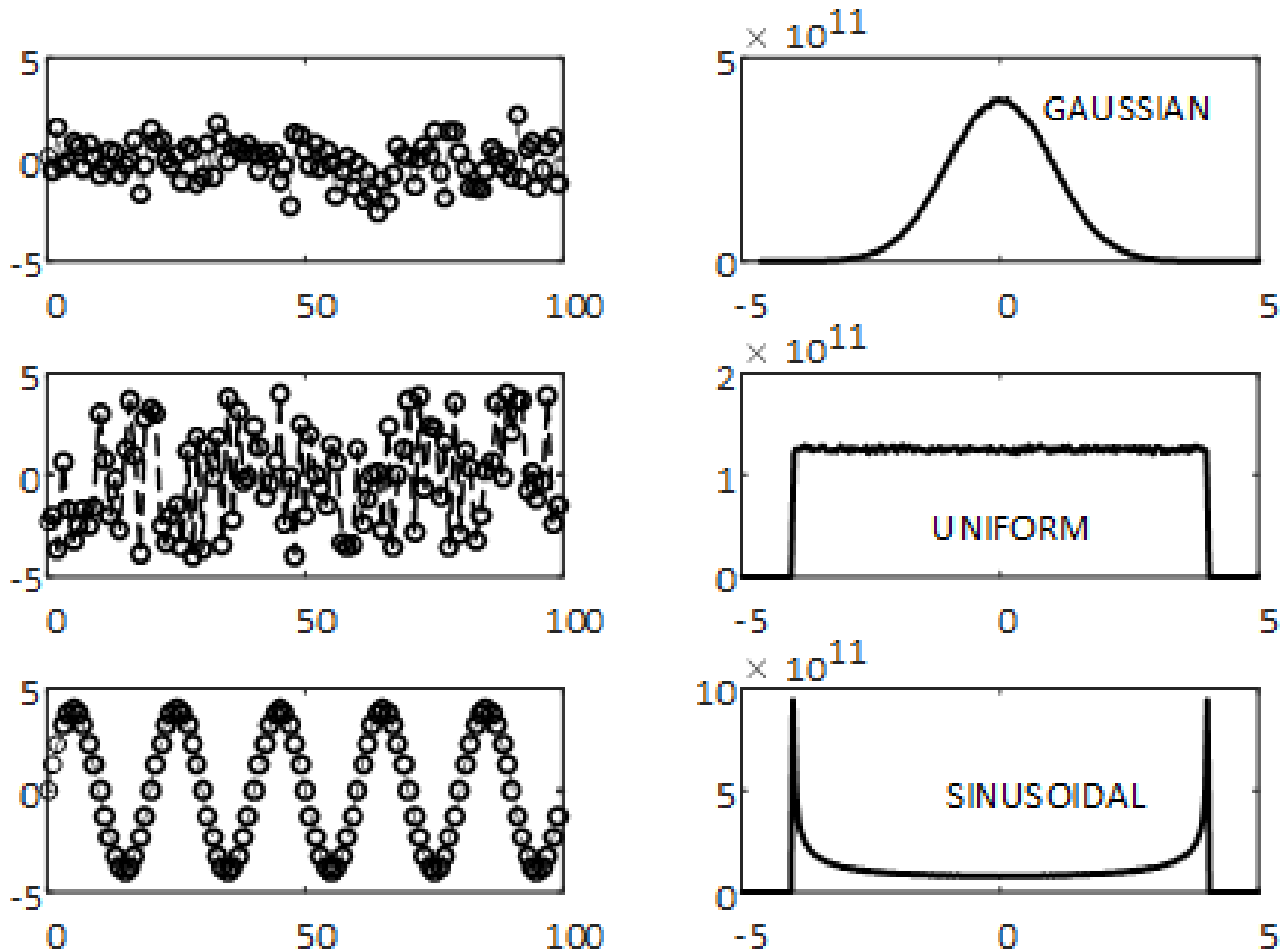
- Plots the number of hits for each jitter amplitude
- Mean, rms, and peak-to-peak jitter can be calculated

Jitter Probability Density Function

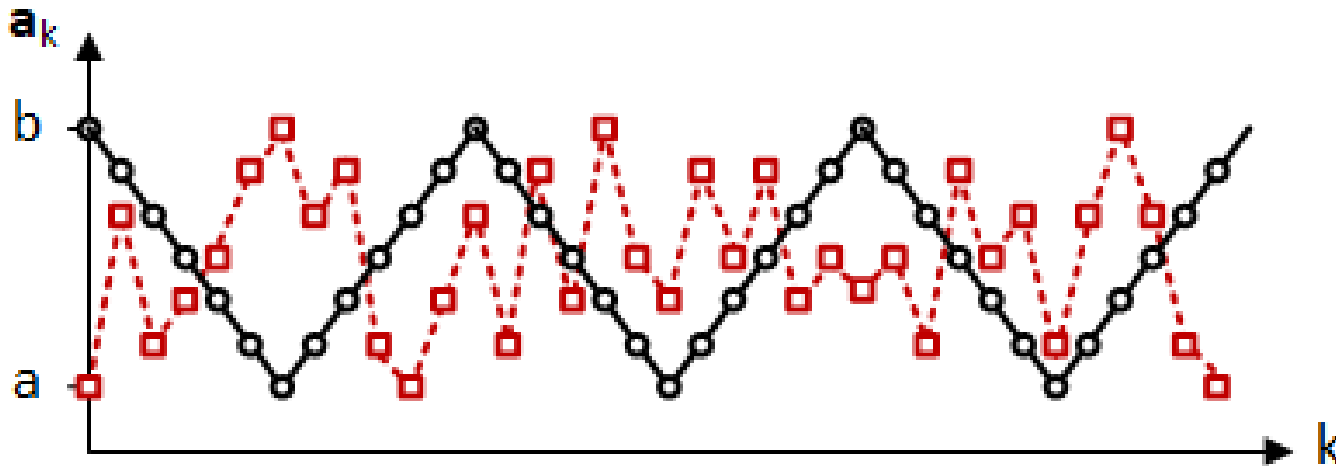


- Normalize vertical axis of histogram to have unit area
- Red area indicates probability of jitter in the interval

Other Histogram Examples

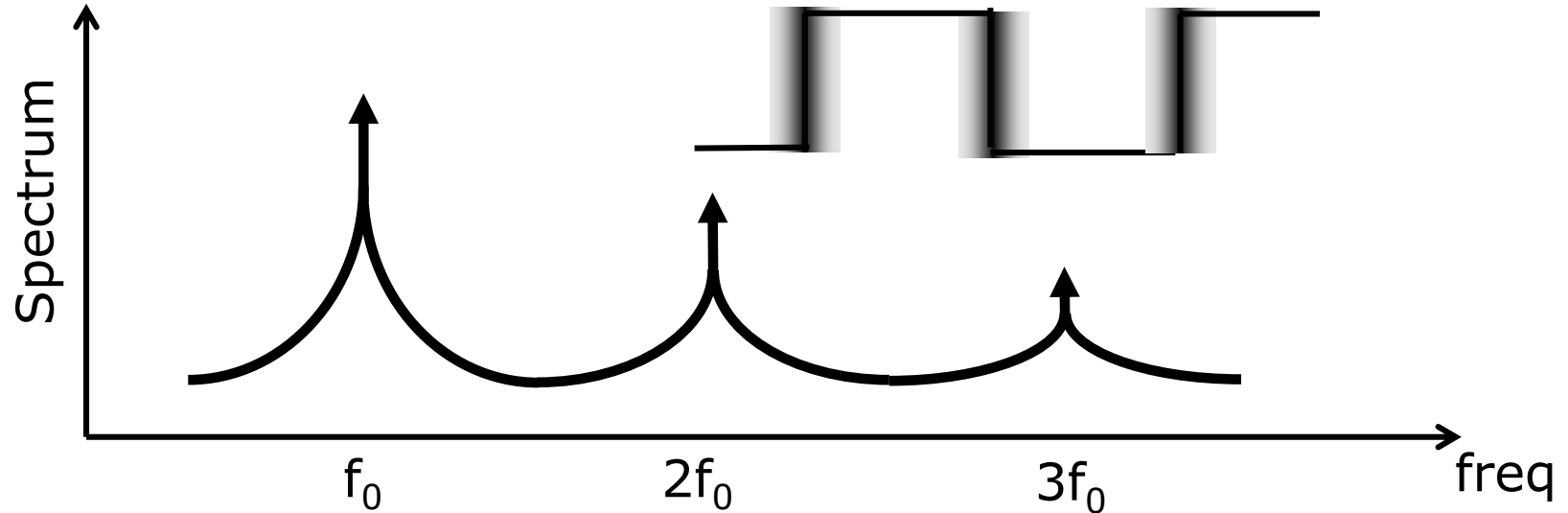


Jitter Histogram/PDF Enough?



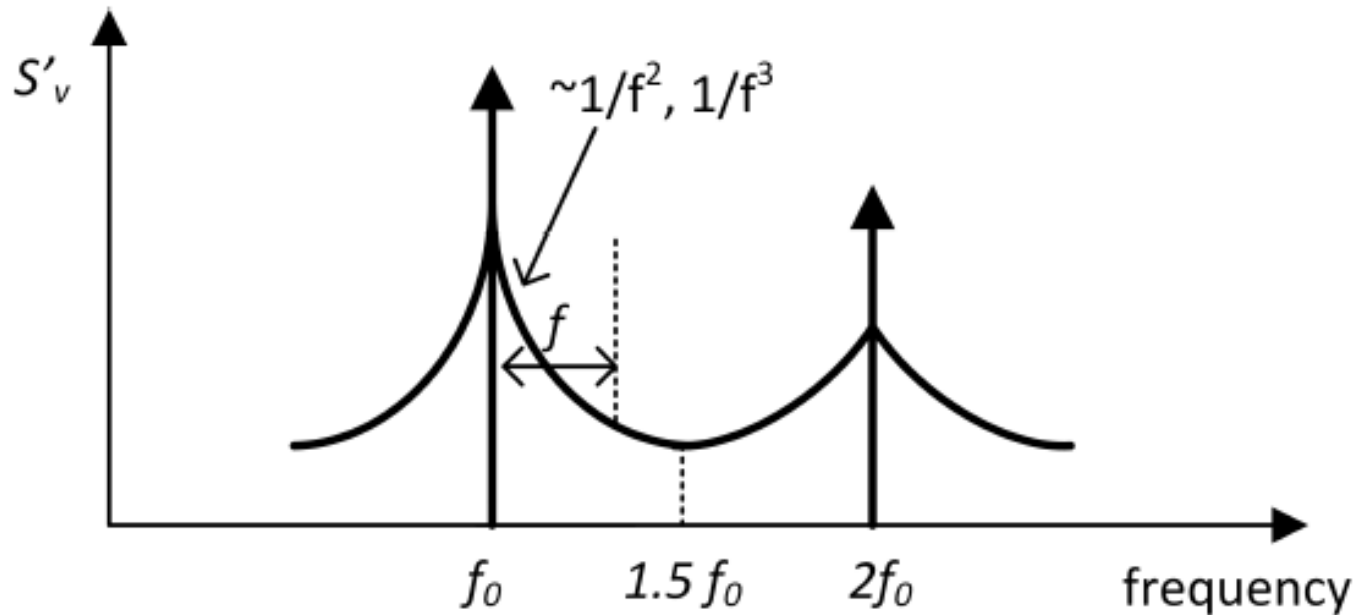
- Histogram or PDF only shows:
 - Relative occurrence of a jitter amplitude (range)
 - But, not the time behavior of jitter
- Two waveforms above have same histogram (uniform)
- But, they have totally different time behavior
 - Black samples are correlated (predictable), red samples not
- Swapping samples in time does not affect the PDF!

Voltage Spectrum of Jittery Clock



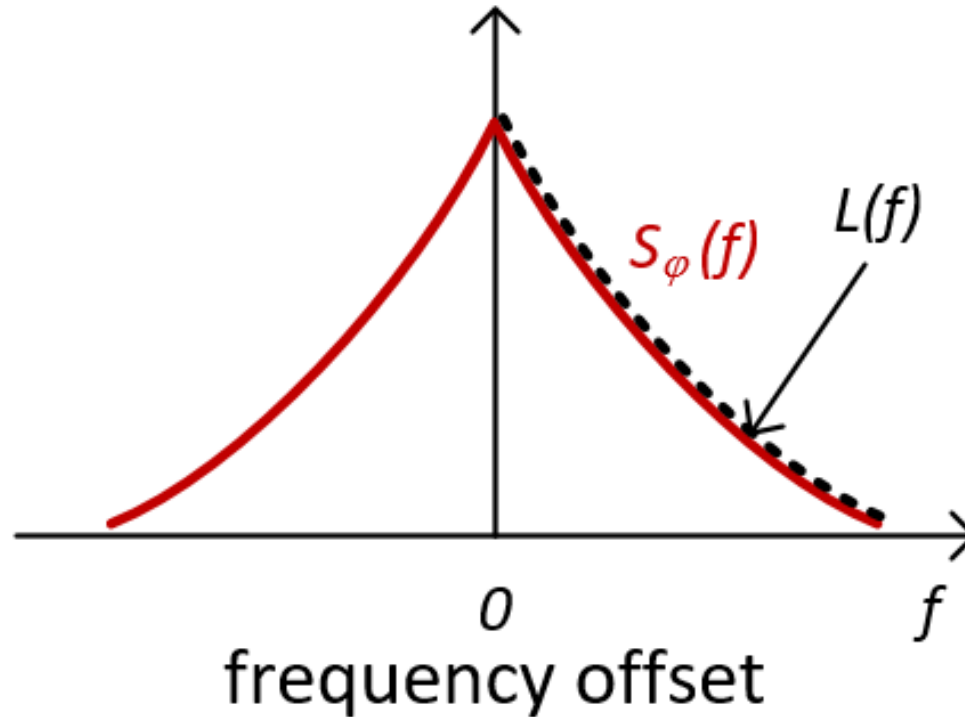
- ❑ Clock is a periodic signal with period $T_0 (=1/f_0)$
- ❑ Clock spectrum will contain harmonics at nf_0
- ❑ In addition, jitter causes “skirts” around delta functions
- ❑ Power level of skirt (relative to carrier power) is called phase noise; typically measured at an offset from f_0
- ❑ Phase noise serves as a figure of merit for the oscillators

Phase Noise



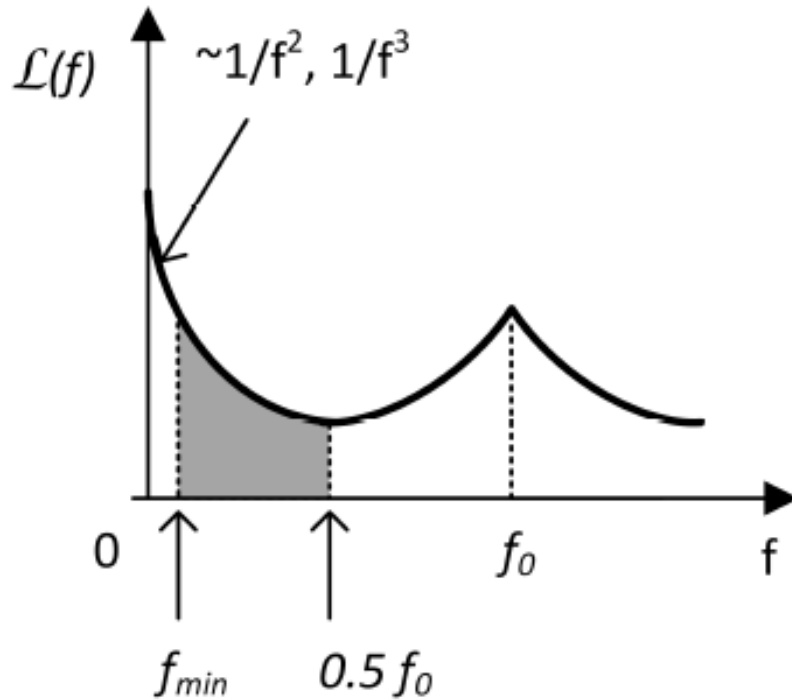
$$\mathcal{L}(f) := \frac{S'_v(f_0 + f) \text{ in 1 Hz bandwidth}}{P}$$

PSD of Jitter



- Can prove PSD of jitter is equal to phase noise
- Note: $\mathcal{L}(f)$ is one-sided whereas $S_{\varphi}(f)$ is two-sided
- $S_{\varphi}(f) = \mathcal{L}(f)u(f) + \mathcal{L}(-f)u(-f)$

From Phase Noise to Jitter rms



$$\varphi = \omega_0 a \quad \sigma_\varphi = \omega_0 \sigma_a$$

$$\frac{a}{T} = \frac{\varphi}{2\pi}$$

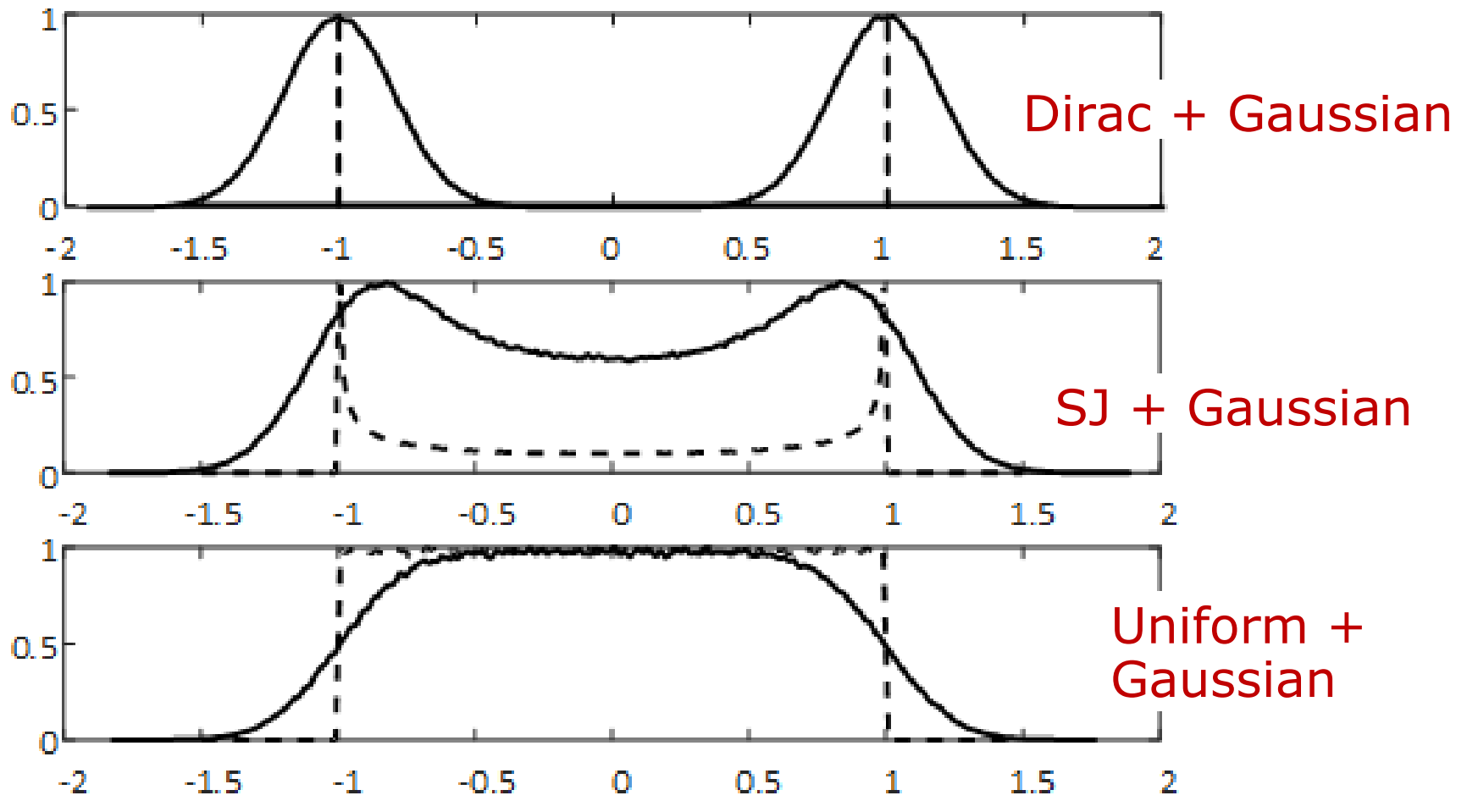
$$\frac{\sigma_a}{T} = \frac{\sigma_\varphi}{2\pi}$$

$$\sigma_a^2 = \int_{-f_0/2}^{+f_0/2} S_a(f) df$$

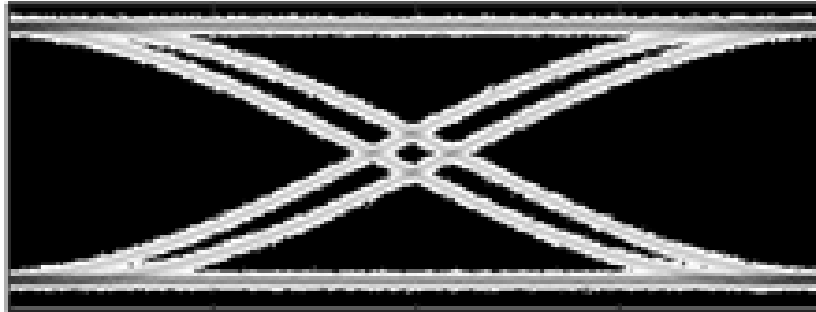
$$\sigma_a = \sqrt{\frac{2}{\omega_0^2} \int_0^{+\infty} \mathcal{L}(f) df}$$

$$\sigma_a = \sqrt{\frac{2}{\omega_0^2} \int_{f_{min}}^{+f_0/2} \mathcal{L}(f) df}$$

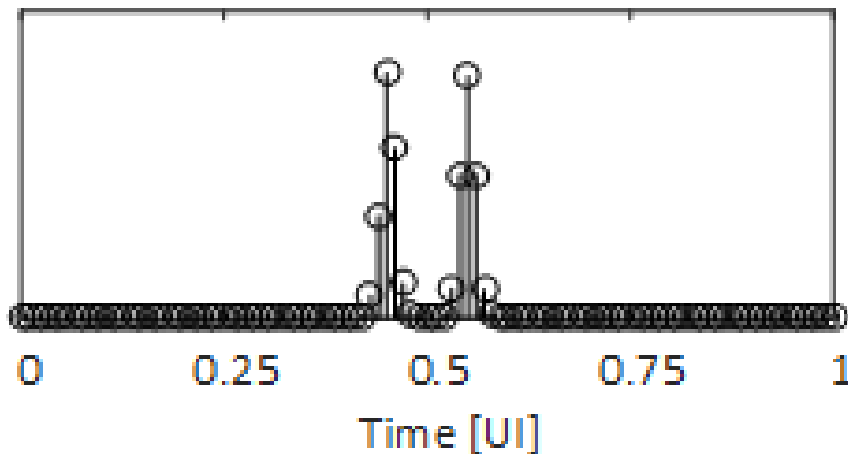
Sum of two jitter: Convolve PDFs



Combined Jitter in Eye Diagram

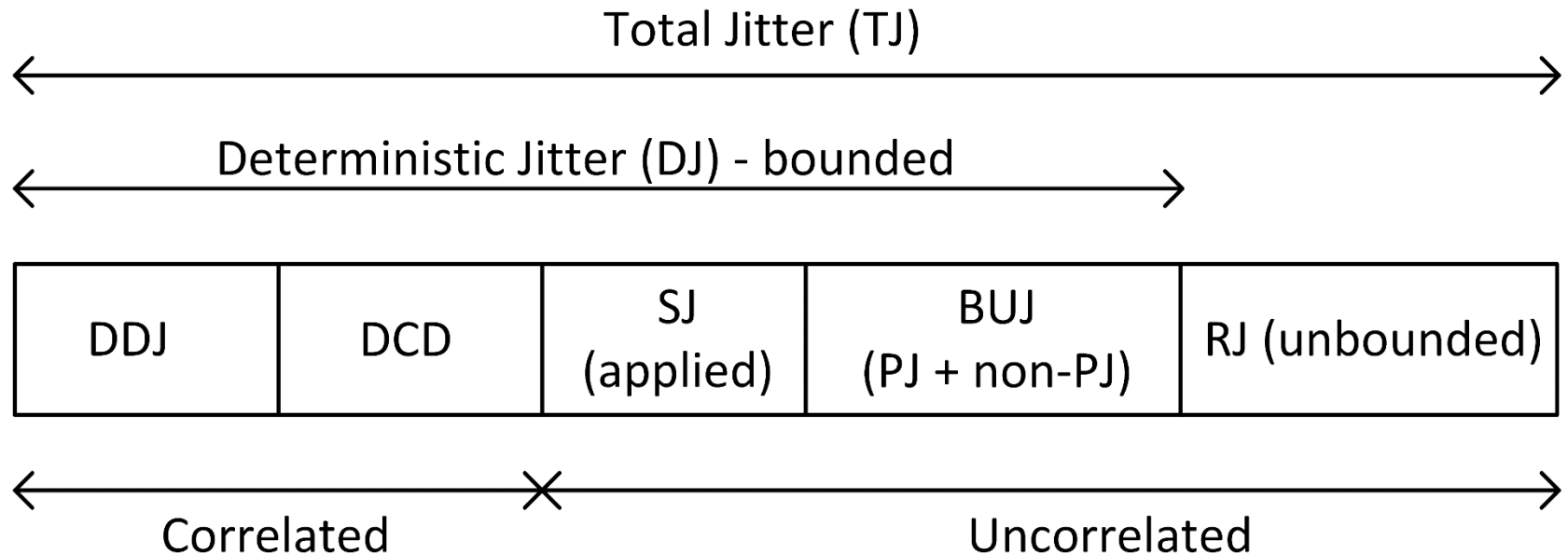


- Combined DCD & RJ
- Convolution of two PDFs



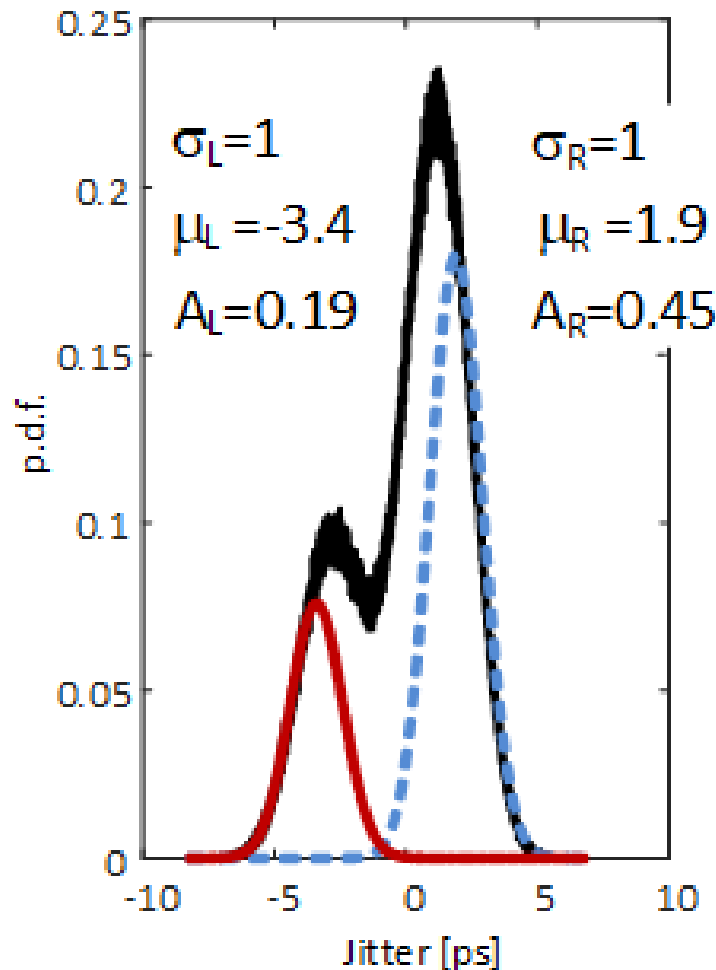
- Combined jitter is sum of individual jitter signals
- Combined jitter PDF is convolution of individual PDFs

Classifying Jitter



- ❑ Total Jitter is sum of DJ and RJ
- ❑ DJ includes:
 - Data-Dependent, Duty-Cycle-Distortion (DCD) Jitter
 - Sinusoidal, any other bounded periodic/non-periodic jitter
- ❑ RJ is unbounded and uncorrelated

Example Calculations



- Tails at two ends
- Fit two tails to two Gaussian
- Calculate Total Jitter (TJ)
- TJ_{pp} for $BER=10^{-12}$

$$TJ_{pp} = DJ_{pp} + RJ_{pp}$$

$$DJ_{pp} = \mu_R - \mu_L = 5.3ps$$

$$RJ_{pp} = RJ_p(L) + RJ_p(R)$$

$$RJ_{pp} = Q\sigma_L + Q\sigma_R = 14ps$$

(assuming $Q=7$)

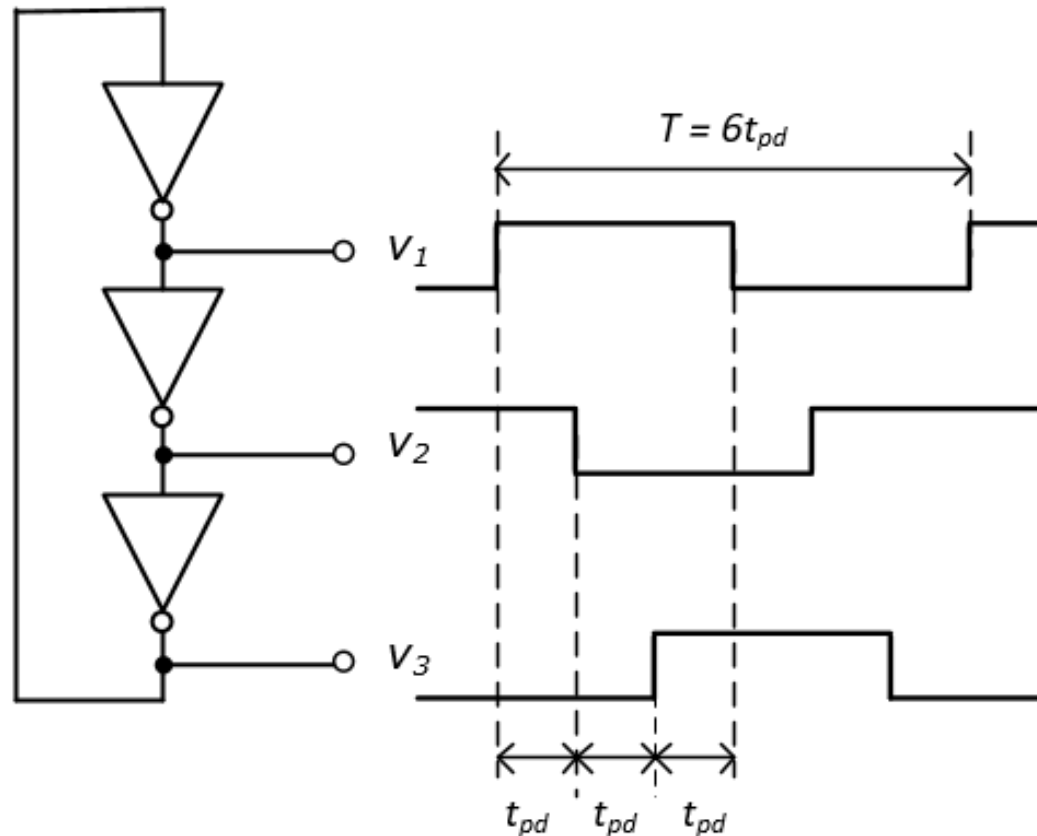
$$TJ_{pp} = 19.3ps$$

$$P(\text{jitter outside } TJ_{pp}) = 0.82e-12$$

Outline

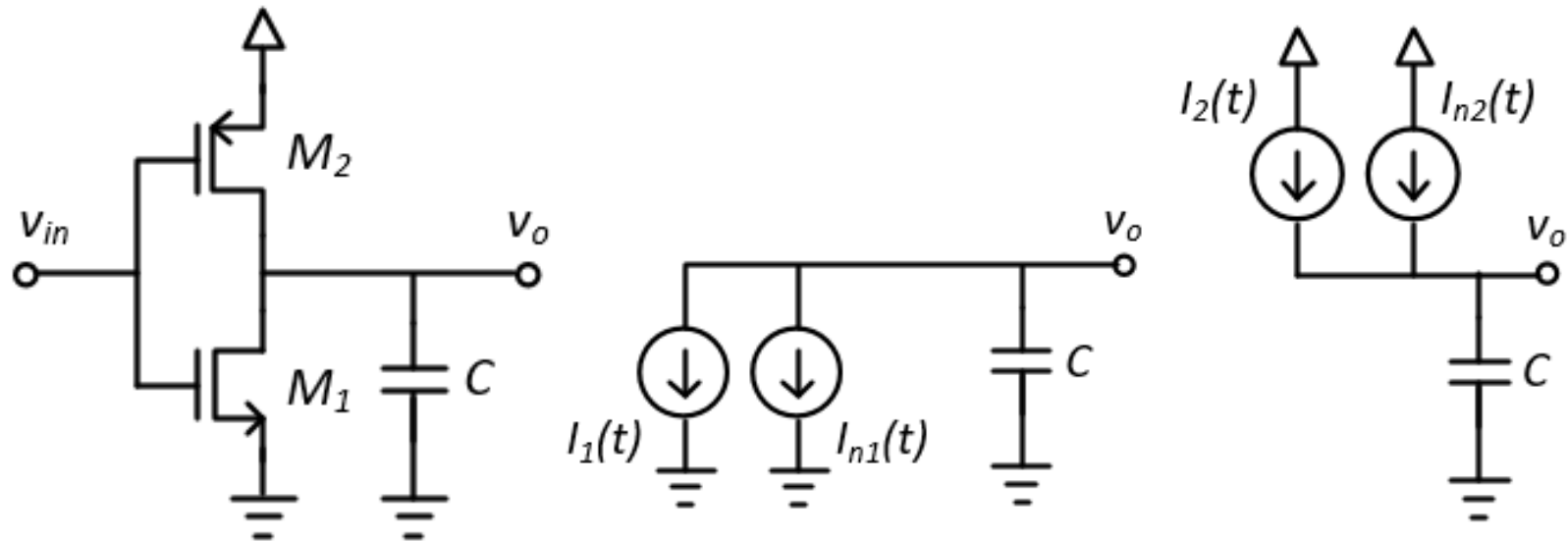
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Example: A Ring Oscillator



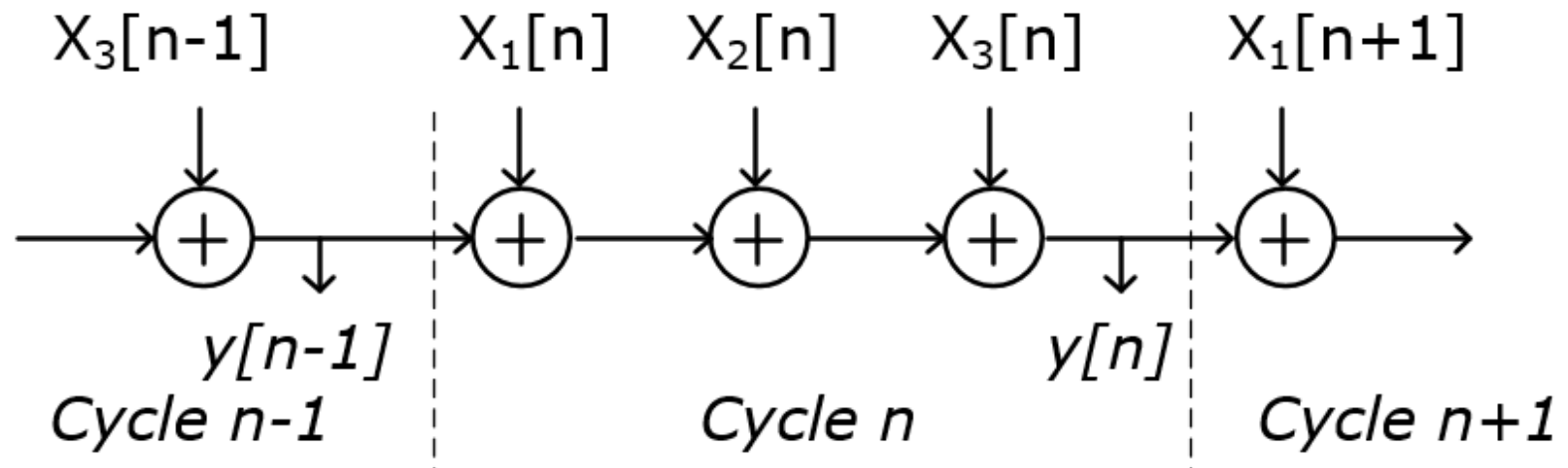
- For any output, say v_1 , the period is $6t_{pd}$
- But t_{pd} is random variable (signal) changing with time

Example: Delay of an Inverter



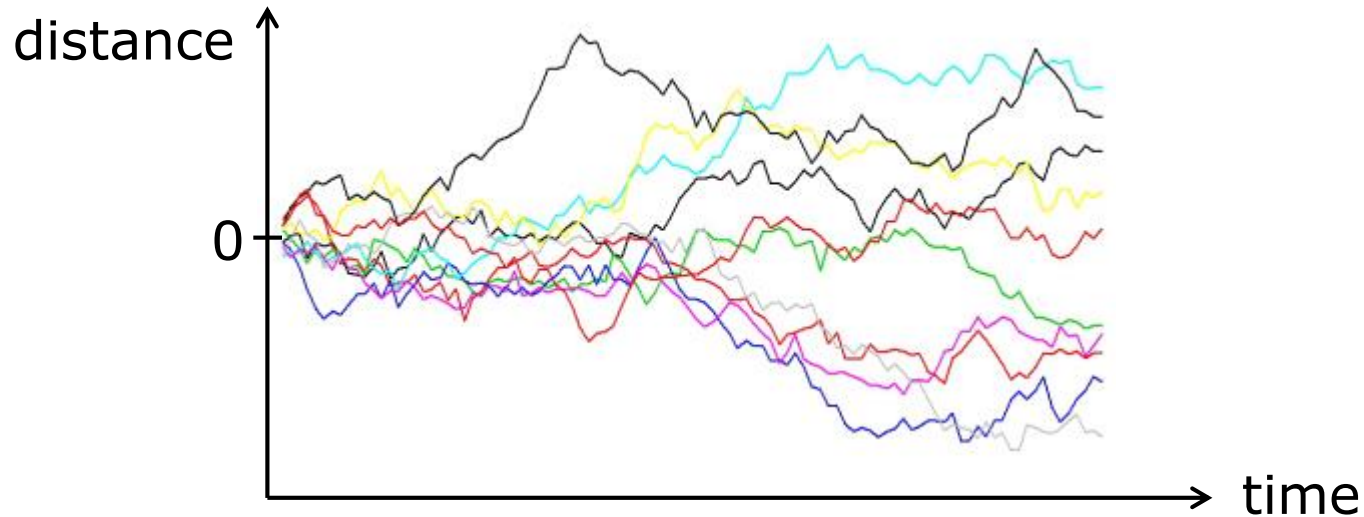
- $I_{n1}(t)$ and $I_{n2}(t)$ represent the thermal (and other) noise currents of M_1 and M_2 , respectively
- $I_{n1}(t)$ and $I_{n2}(t)$ will cause v_o to reach a threshold ($V_{DD}/2$) faster or slower than nominal; causing delay of each stage to be a random variable

Modeling Jitter in Ring Oscillator



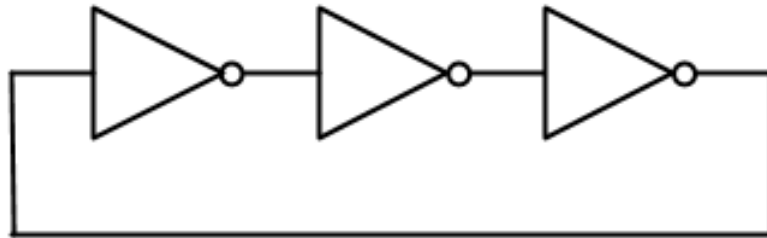
- ❑ Let $X_i[n]$ represent the random *excess delay* introduced by inverter i in n -th cycle
- ❑ $X_i[n]$ is a random signal with expected value of zero
- ❑ What can we say about the jitter in the output $y[n]$?
- ❑ $y[n] = y[n-1] + X_1[n] + X_2[n] + X_3[n]$
- ❑ Reasonable to assume $X_i[n]$ is stationary & uncorrelated
- ❑ Then, $y[n]$ shows characteristics of a *random walk*

Random Walk Process

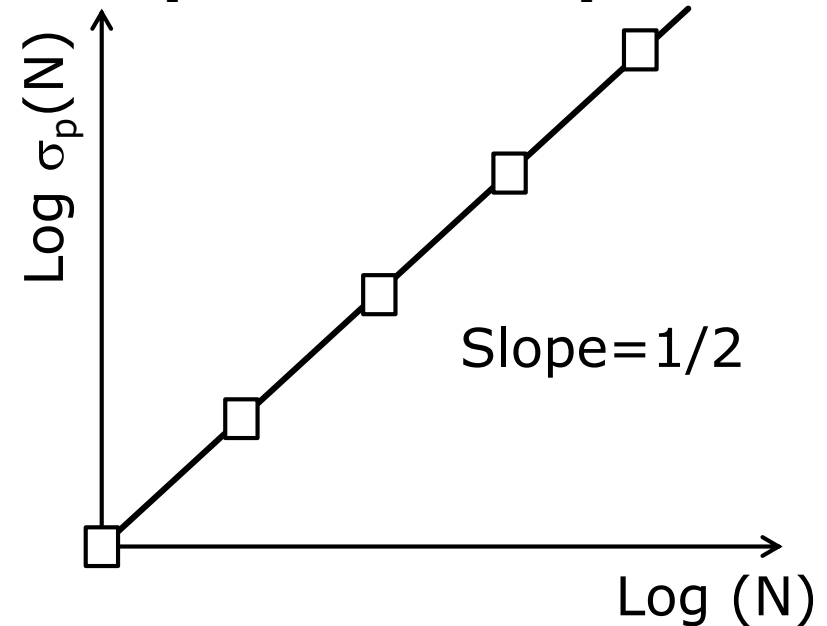


- Start at 0 and toss a coin
 - If head, move one step forward, then repeat
 - If tail, move one step backward, then repeat
- Graph shows 10 different trials (imagine for 10 people)
- The *expected* distance for all trials are zero
- But the variation around 0 grows over time

Jitter Variance over Time



[McNeill JSSC 1997]

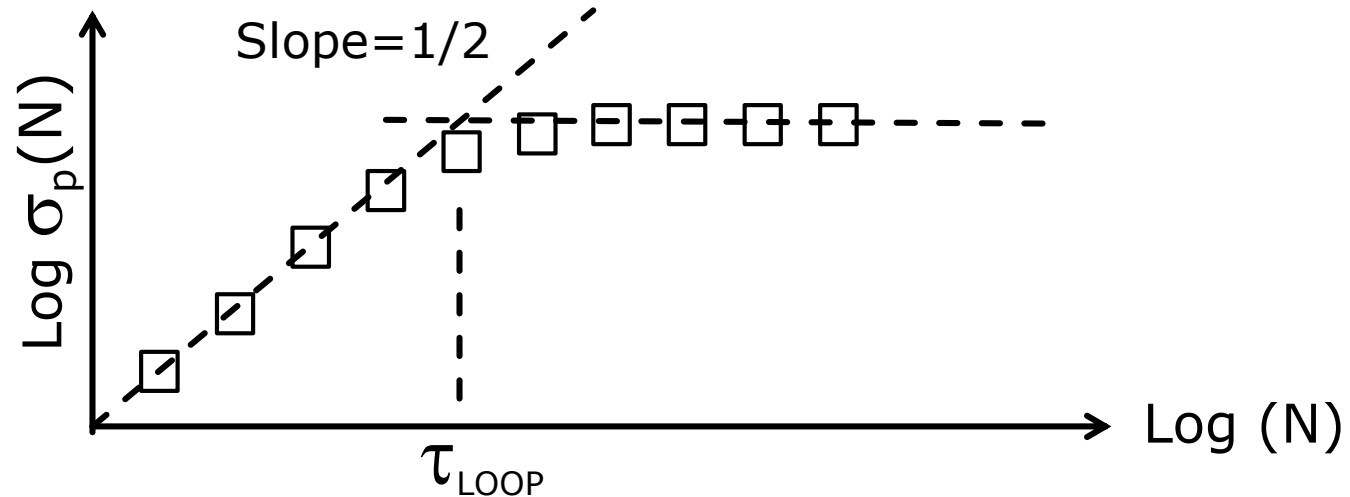


$$\sigma_p(N) = \sqrt{N} \sigma_p(1)$$

$$\text{Log}(\sigma_p(N)) = \text{Log}(\sigma_p(1)) + \frac{1}{2} \text{Log}(N)$$

- Jitter variance increases linearly with time
- Jitter rms increases with root square of time

Jitter Variance of a PLL



- ❑ Oscillator can be placed inside a PLL loop to compare its timing against a clean reference clock
- ❑ Jitter variance increase with time until one loop delay, at which point jitter variance no longer grows

Summary of Part One

- Jitter definitions:
 - Absolute jitter: deviation from an ideal clock timing
 - Relative jitter: timing difference between two real clocks
 - Period jitter: deviation in period from average period

- Jitter histogram, PDF, PSD
 - Histogram/PDF provide statistics: mean, rms, peak-to-peak
 - PSD is based on jitter behavior over time (autocorrelation)
 - PSD provides information in frequency domain

- Jitter variance in a ring increases linearly with time

- A control loop (in a PLL) is used to limit jitter

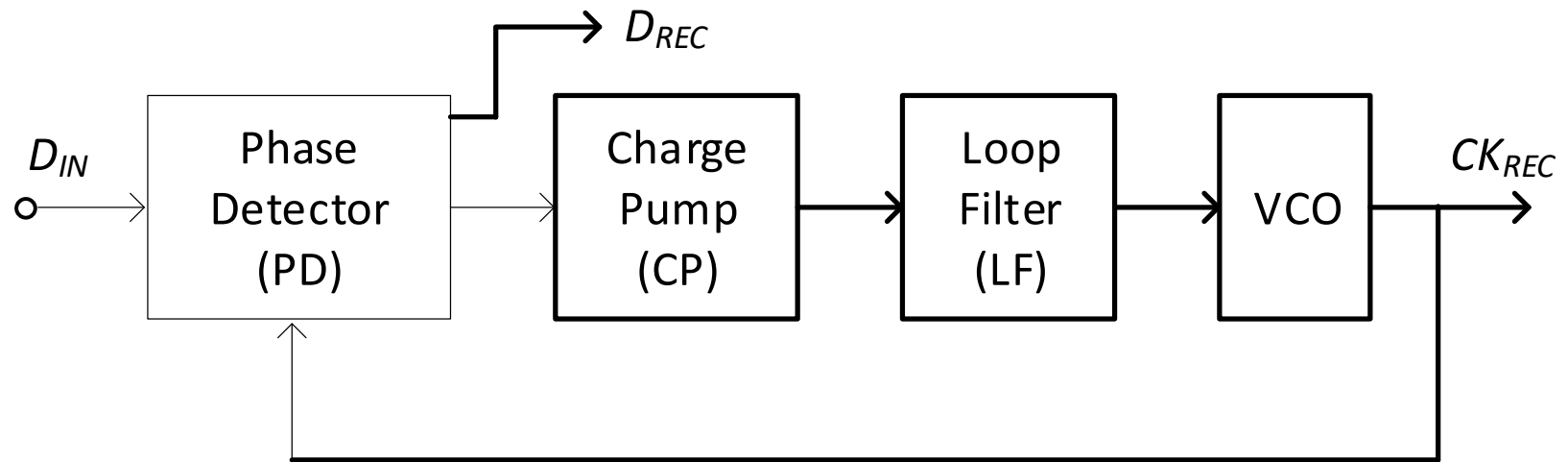
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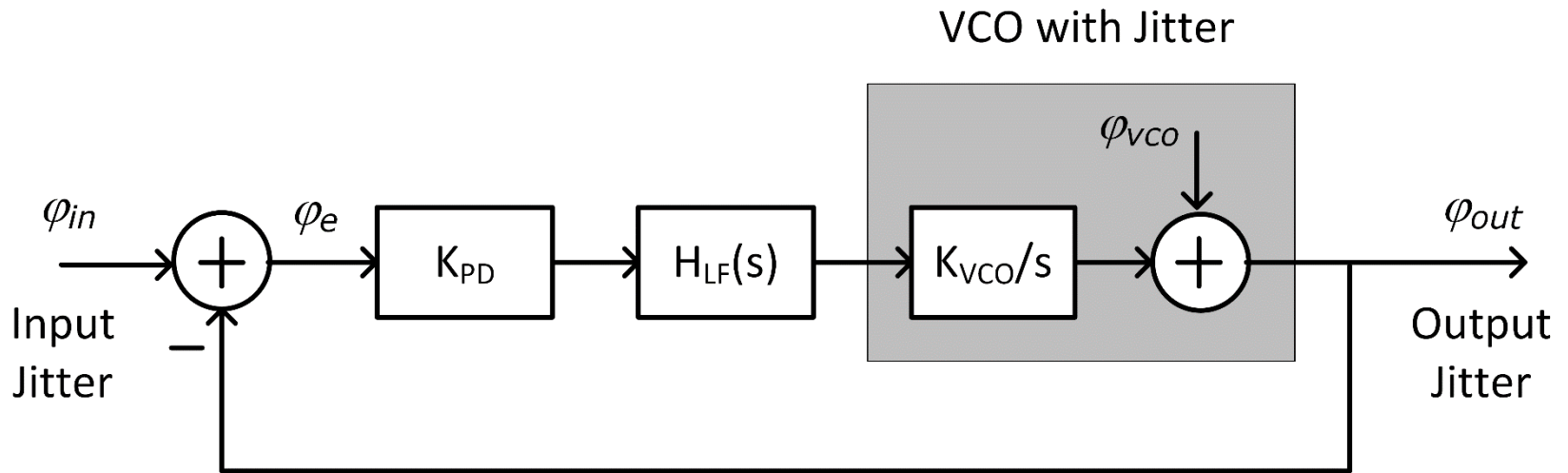
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Clock and Data Recovery Blocks



- ❑ A loop measures the phase difference between D_{IN} and CK_{REC} and controls the VCO frequency
- ❑ Loop dynamics shaped by PD, CP, LF, and VCO behavior
- ❑ CK_{REC} is used to sample D_{IN} and produce D_{REC}

Linear Model of CDR

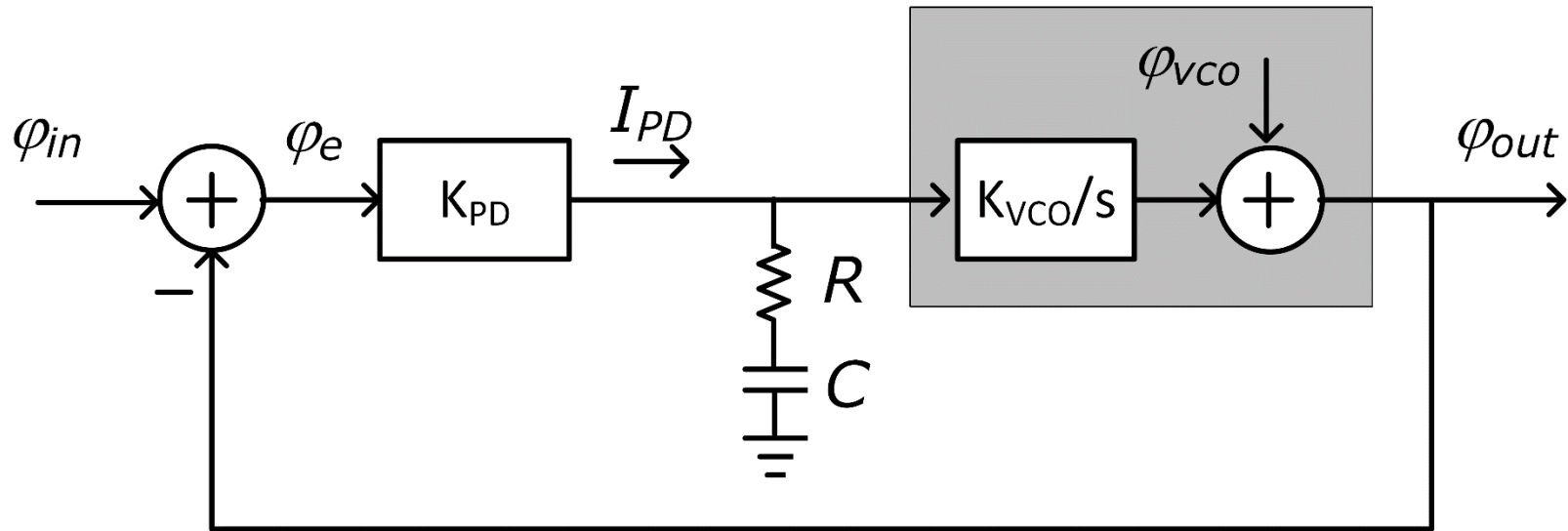


$$S_{out}(f) = |H_T(f)|^2 S_{in}(f) + |H_G(f)|^2 S_{VCO}(f)$$

$$|H_T(f)|^2 = \left| \frac{K_{PD} K_{VCO} H_{LF}(f)}{j2\pi f + K_{PD} K_{VCO} H_{LF}(f)} \right|^2$$

$$|H_G(f)|^2 = \left| \frac{j2\pi f}{j2\pi f + K_{PD} K_{VCO} H_{LF}(f)} \right|^2$$

Model of CDR with Charge Pump



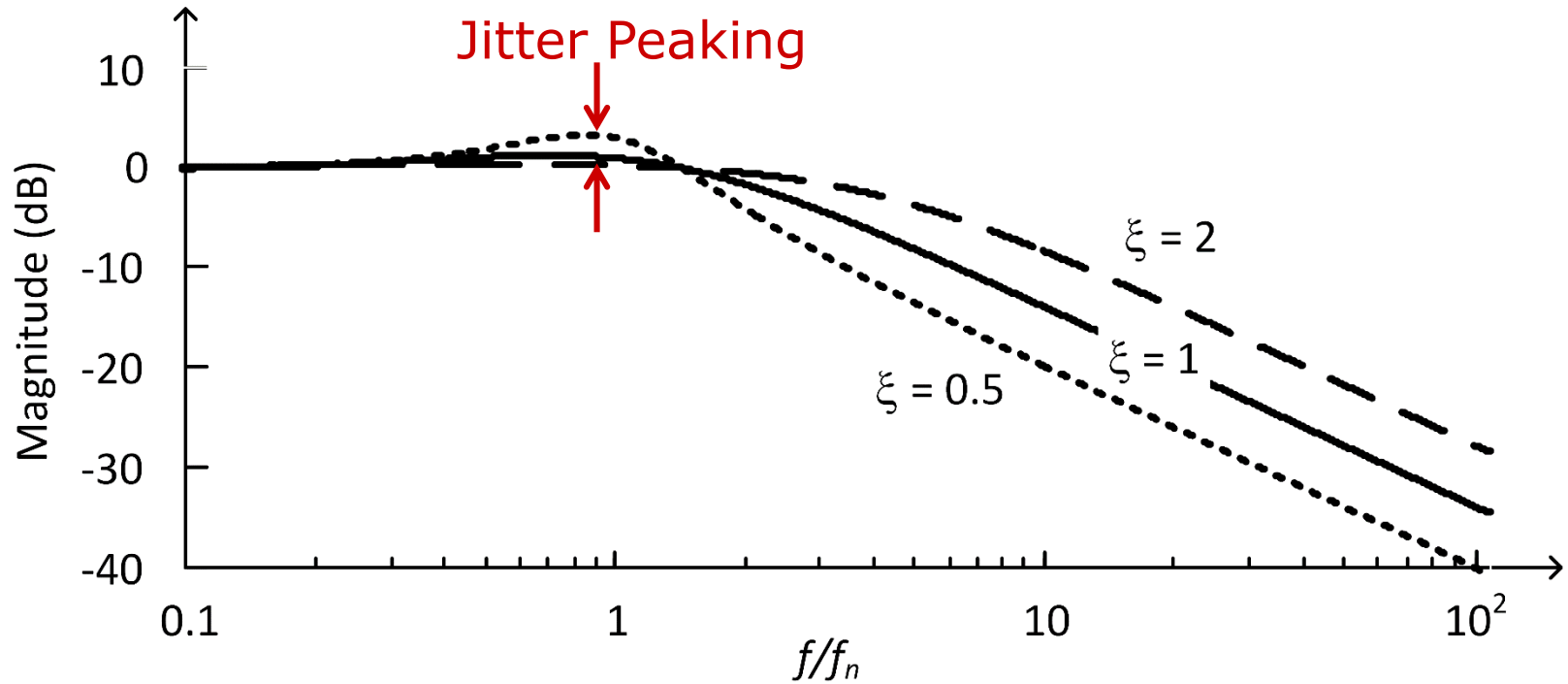
$$H_T(s) = \frac{2\xi\omega_n s + \omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2}$$

$$\omega_n^2 := \frac{K_{PD}K_{VCO}}{C}$$

$$|H_T(f)|^2 = \frac{4\xi^2\omega_n^2\omega^2 + \omega_n^4}{(\omega_n^2 - \omega^2)^2 + 4\xi^2\omega_n^2\omega^2}$$

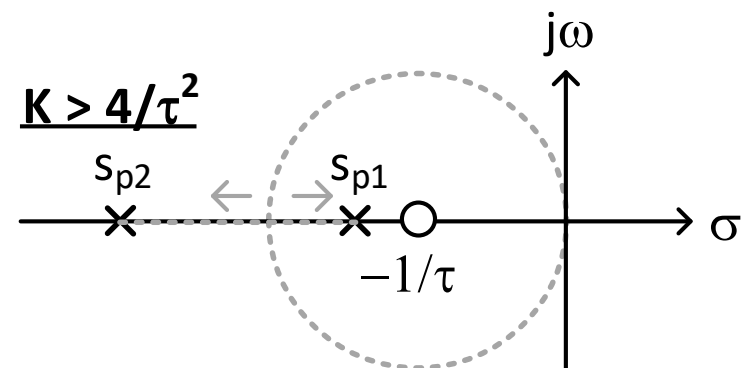
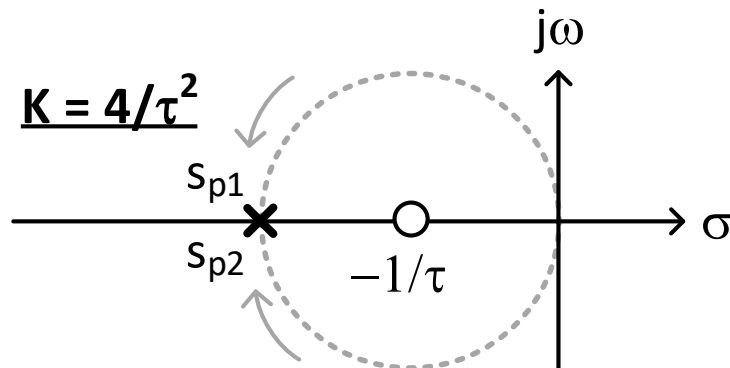
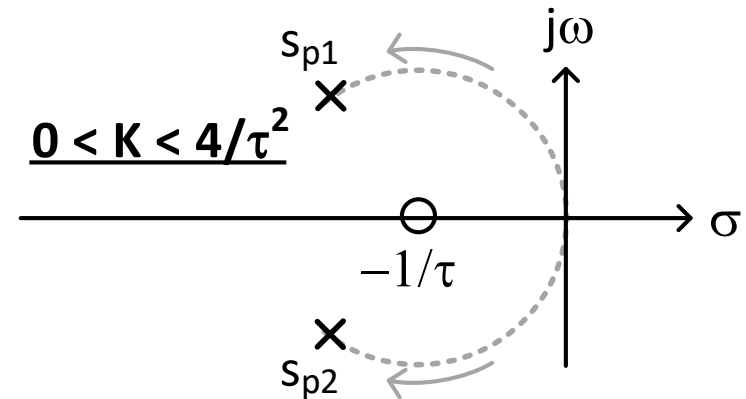
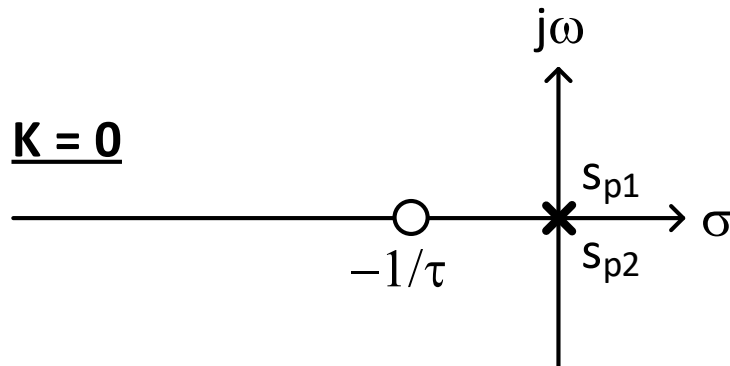
$$\xi := \frac{K_{PD}K_{VCO}R}{2\omega_n}$$

Jitter Transfer Function

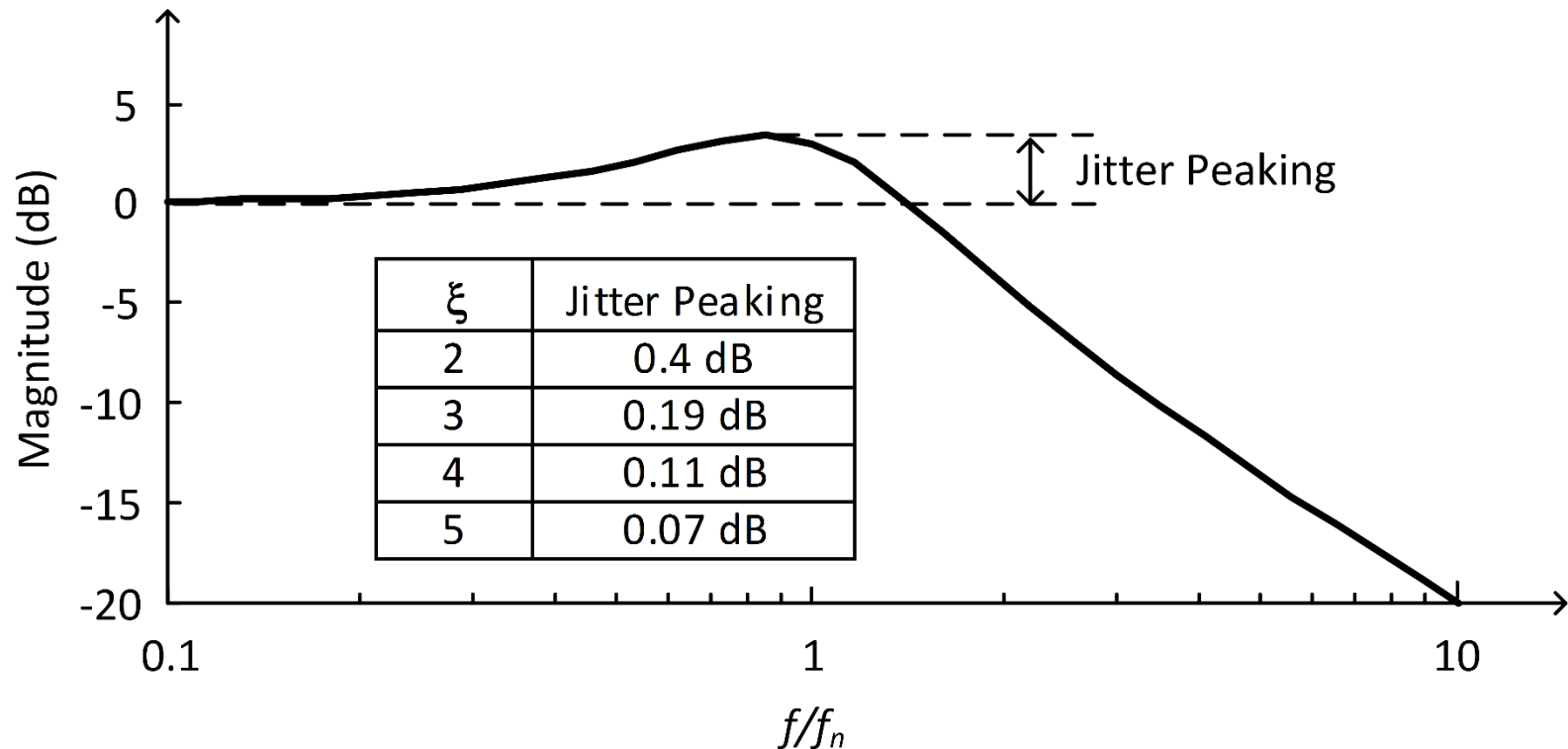


$$|H_T(f)|^2 = \begin{cases} 1 & \text{if } f \ll f_n \\ 4\xi^2 \left(\frac{f_n}{f}\right)^2 & \text{if } f \gg f_n \end{cases}$$

Zero/Pole Locations

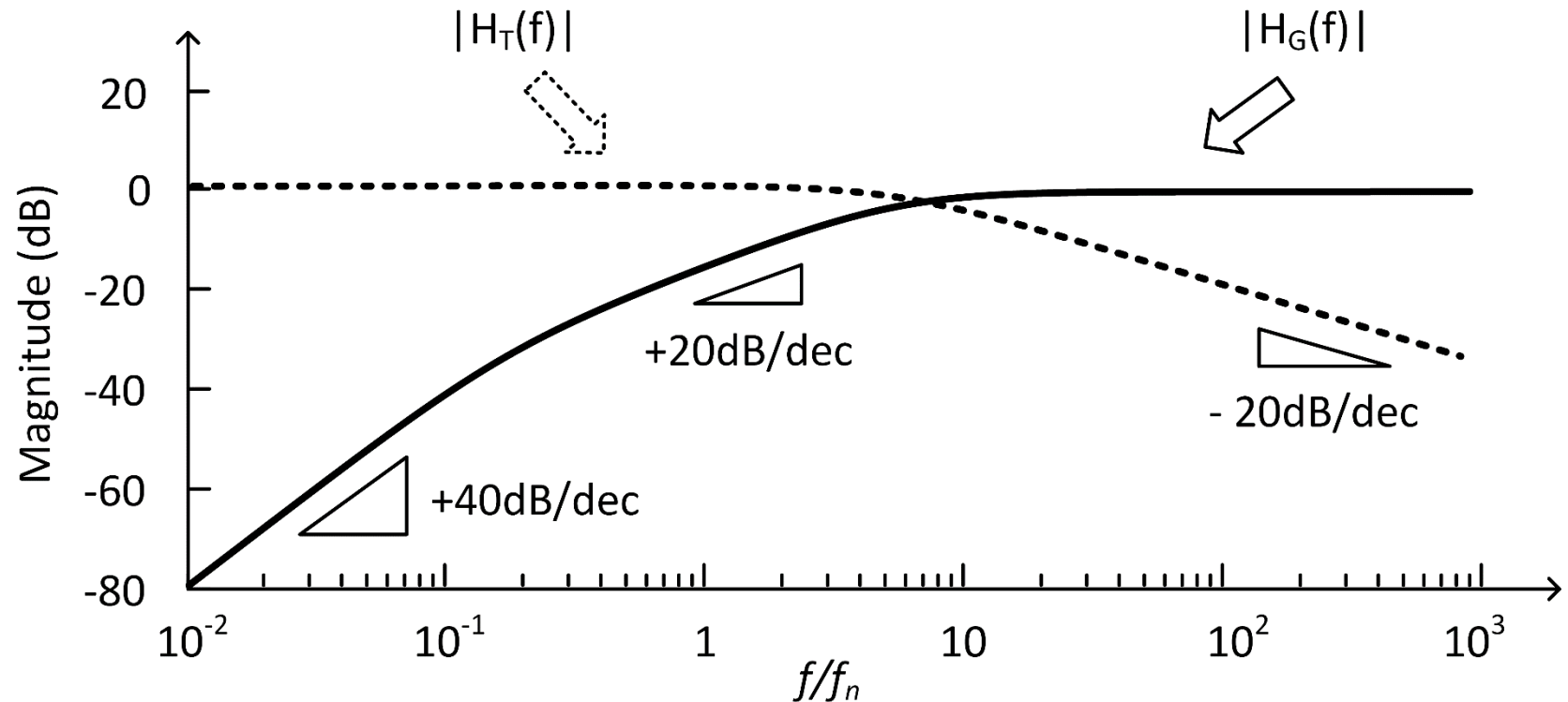


Jitter Peaking



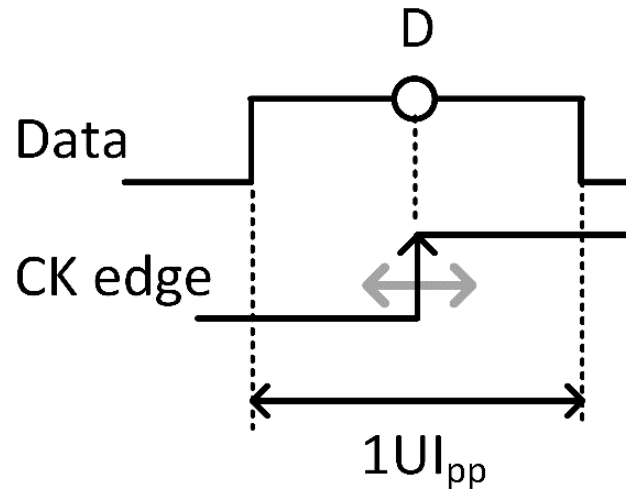
- ❑ Undesirable as it enhances jitter, esp. in repeaters
- ❑ Standards requirement $< 0.1\text{dB}$

Jitter Generation Function



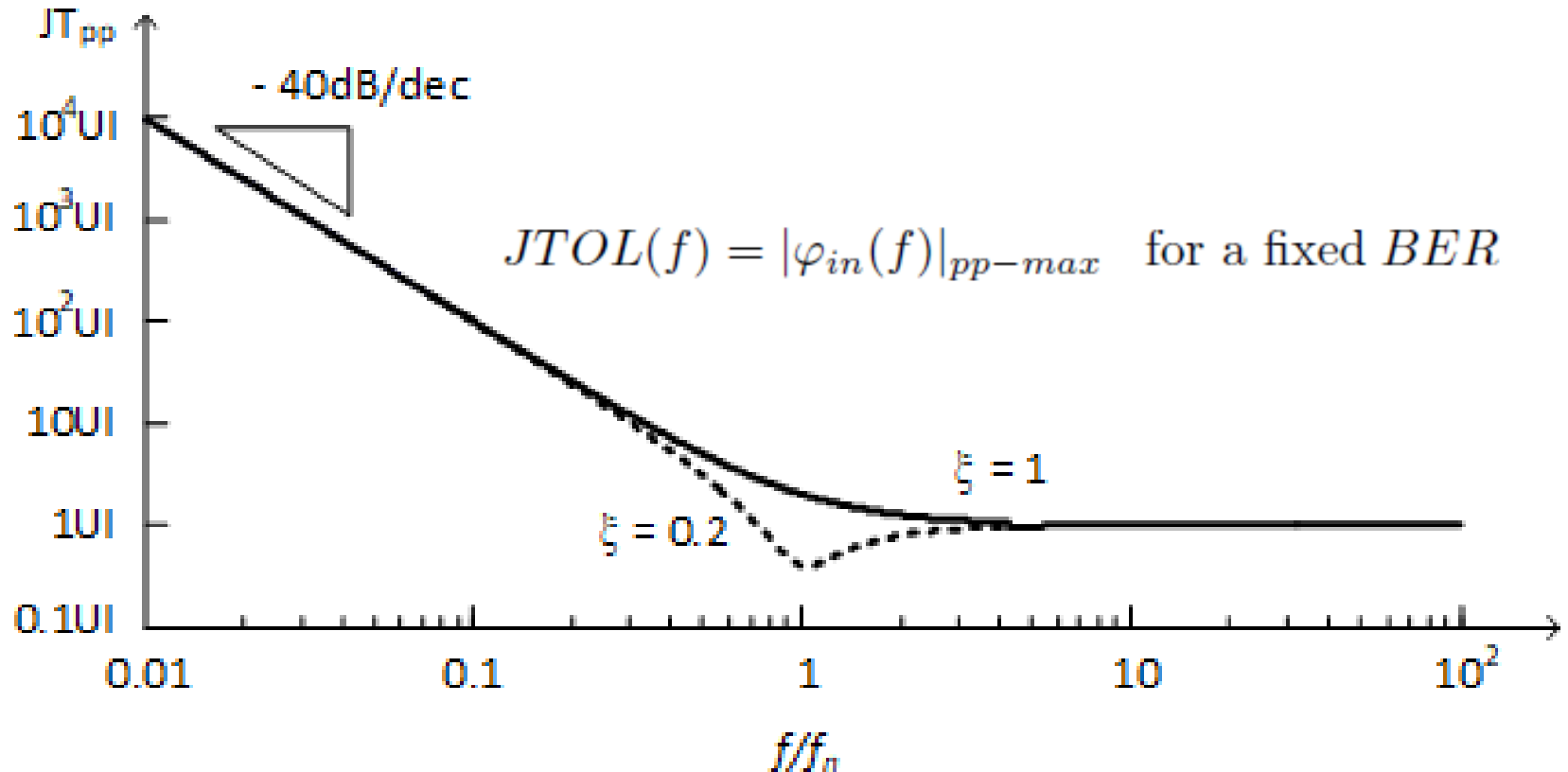
$$|H_G(f)|^2 = \frac{\omega^4}{(\omega_n^2 - \omega^2)^2 + 4\xi^2\omega_n^2\omega^2}$$

Jitter Tolerance Concept



- ❑ Maximum tolerable peak-to-peak jitter on CK edge
- ❑ $1UI_{pp}$ for high jitter frequencies
- ❑ Higher than $1UI_{pp}$ for lower jitter frequencies

Jitter Tolerance Curve



$$JTOL(f) = \left| \frac{\varphi_{in}(f)}{\varphi_e(f)} \right| [UI] \quad JTOL(f) = \begin{cases} \left(\frac{f_n}{f} \right)^2 & \text{if } f \ll f_n \\ 1 & \text{if } f \gg f_n \end{cases}$$

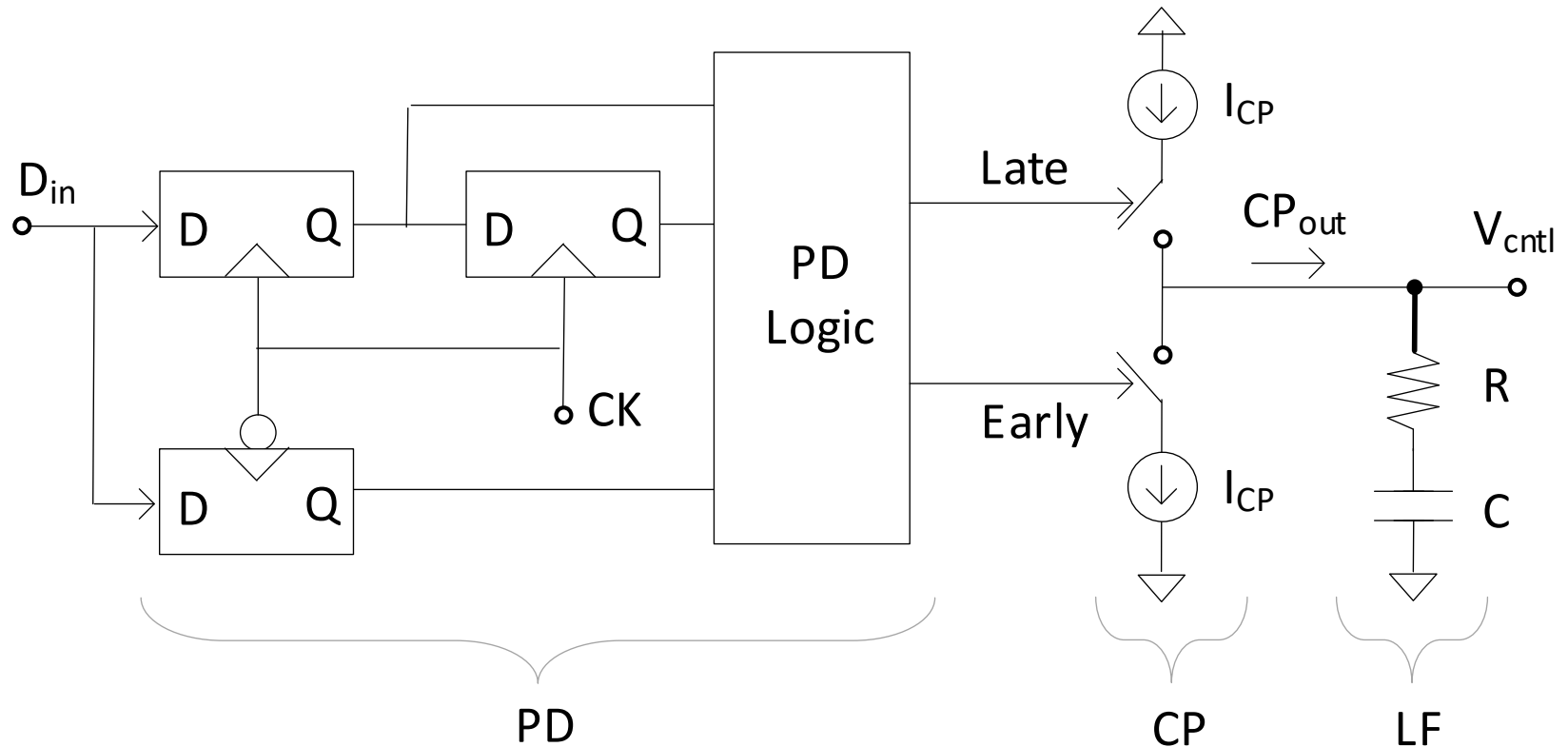
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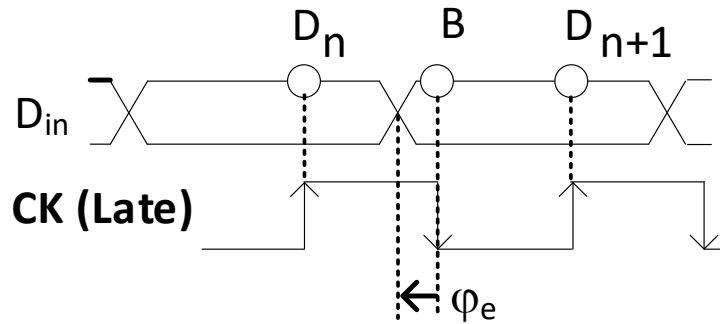
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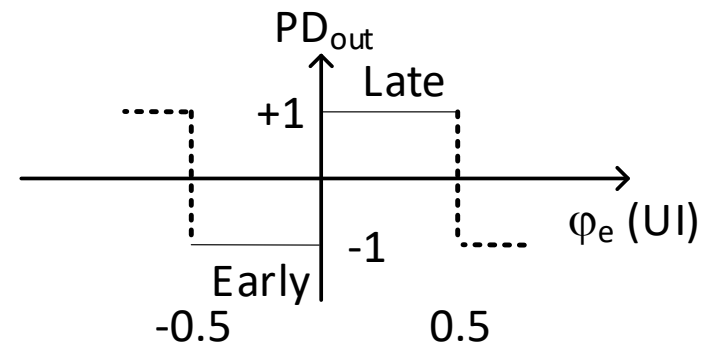
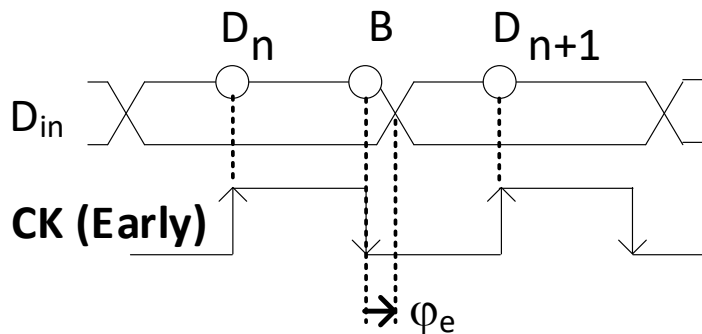
Bang-Bang PD Operation (1 of 3)



Bang-Bang PD Operation (2 of 3)

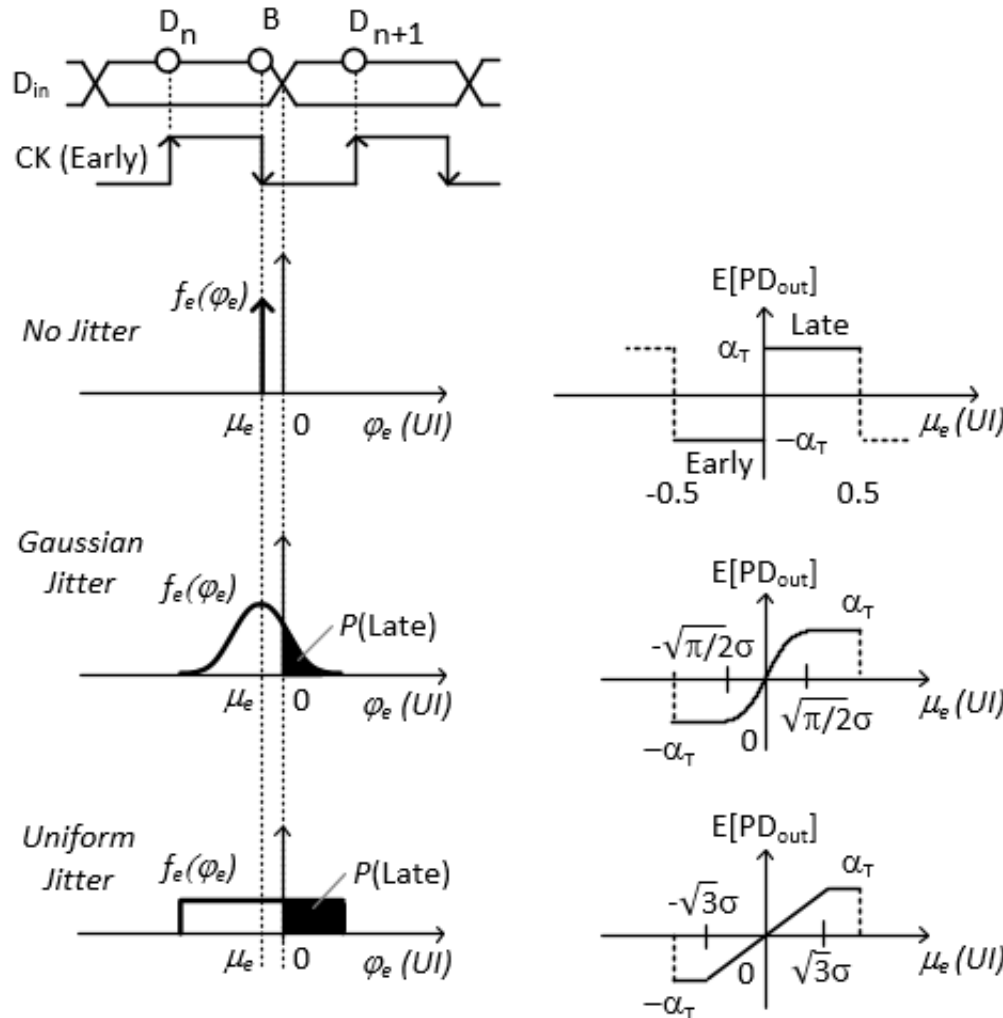


D_n	B	D_{n+1}	Early	Late	PDout
X	$\bar{X}$	$\bar{X}$	0	1	1
X	X	$\bar{X}$	1	0	-1
X	X	X	0	0	0



Bang-Bang PD Operation (3 of 3)

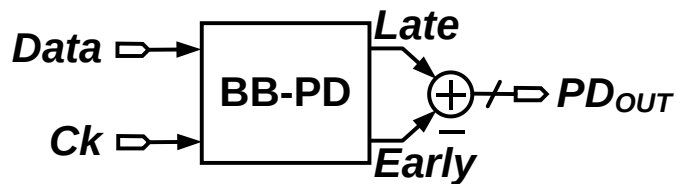
[Lee JSSC 2004]



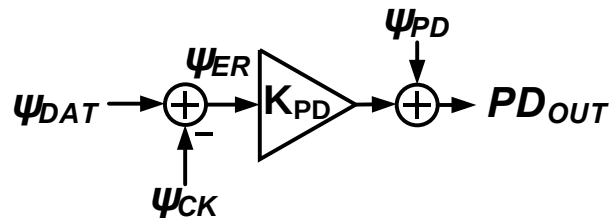
BB-PD Model with Jitter

[Liang JSSC 2015]

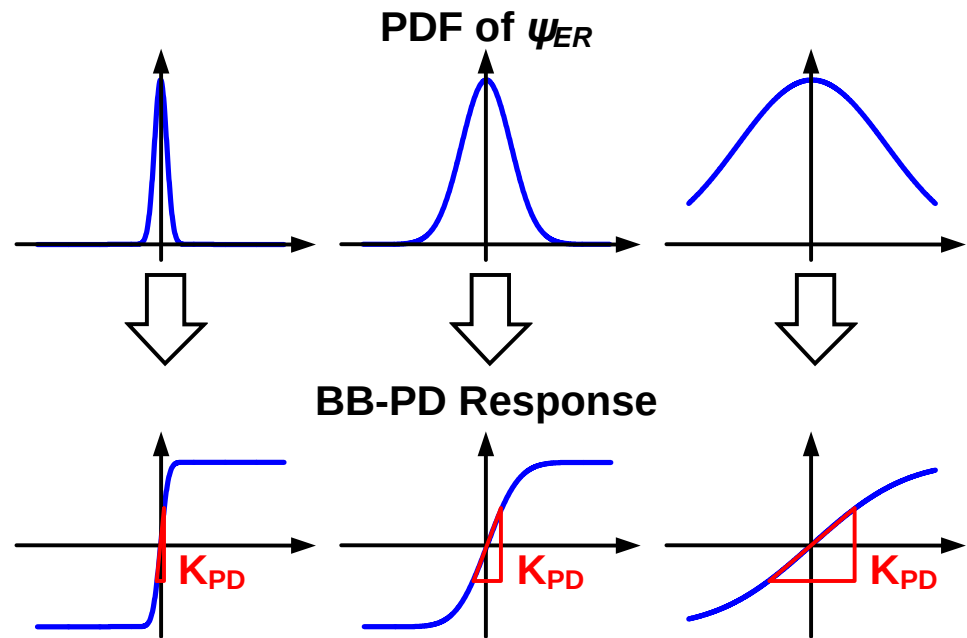
Linear Model of BB-PD



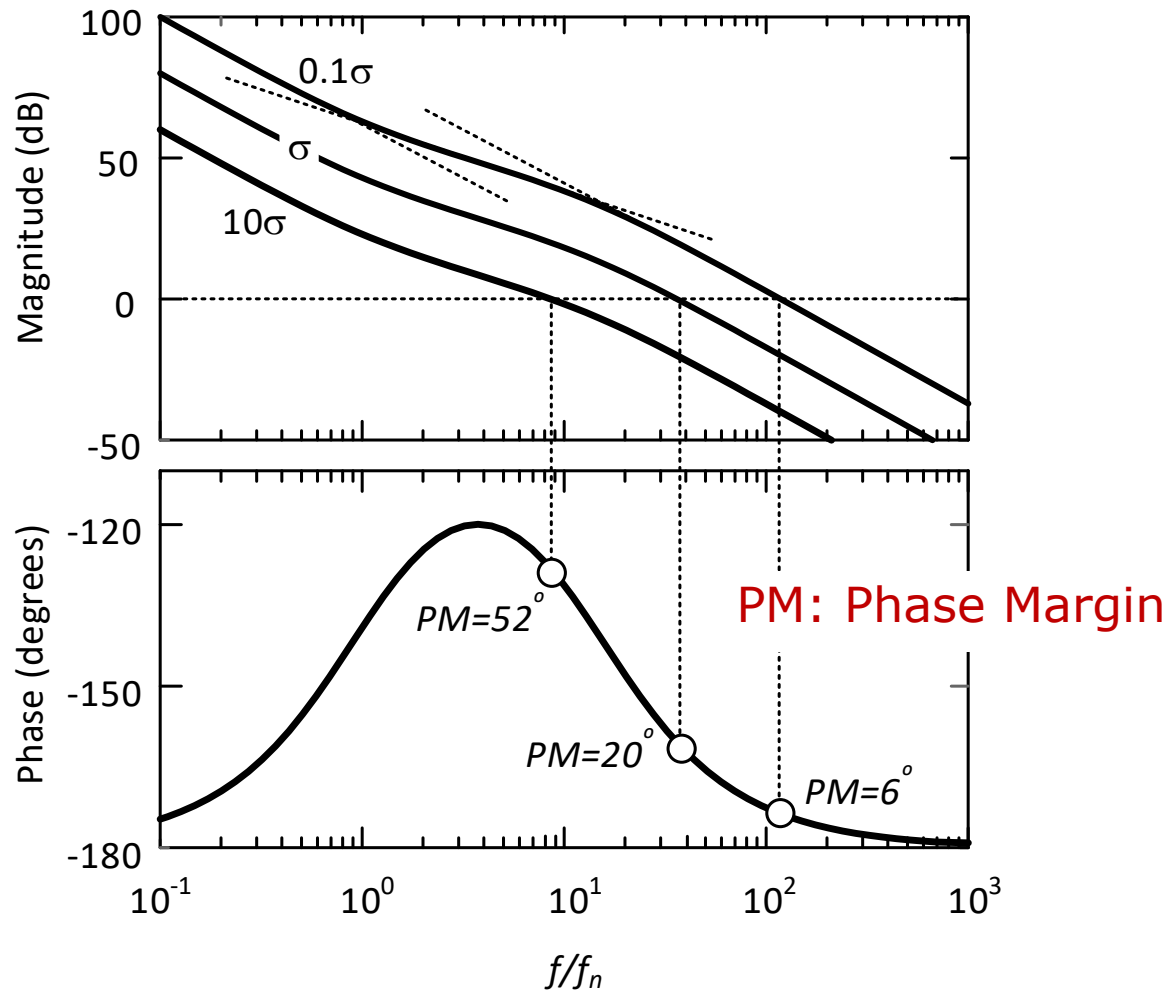
Linear Model



Effect of ψ_{ER} on PD Gain



Effects of Jitter on CDR Stability



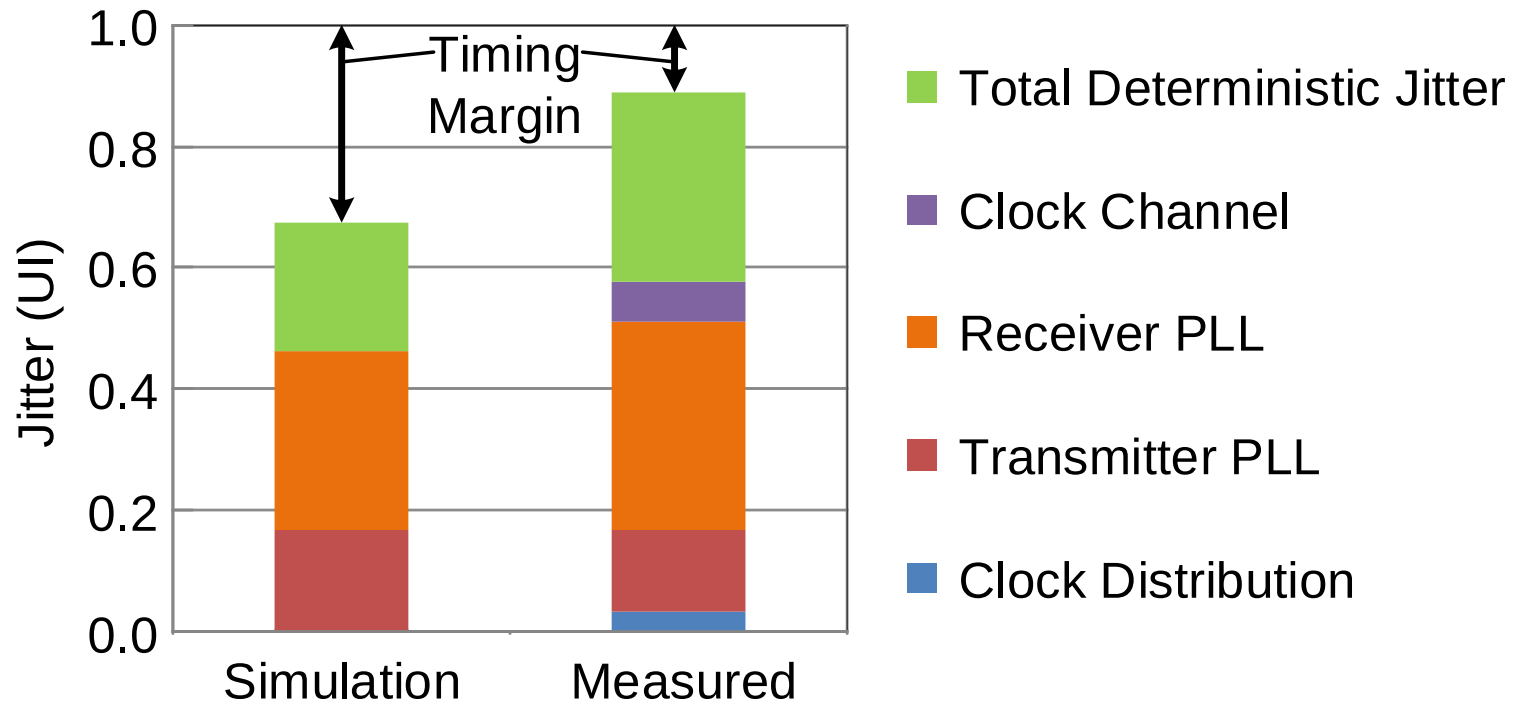
Outline

- Motivation
- Jitter Definitions: What is Jitter?
- Characterizing and Classifying Jitter
- Example: Jitter in Ring Oscillator
- Example: Jitter in Clock and Data Recovery
- Effects of Jitter on Bang-Bang CDR Operation

- Jitter Monitoring and Jitter Mitigation

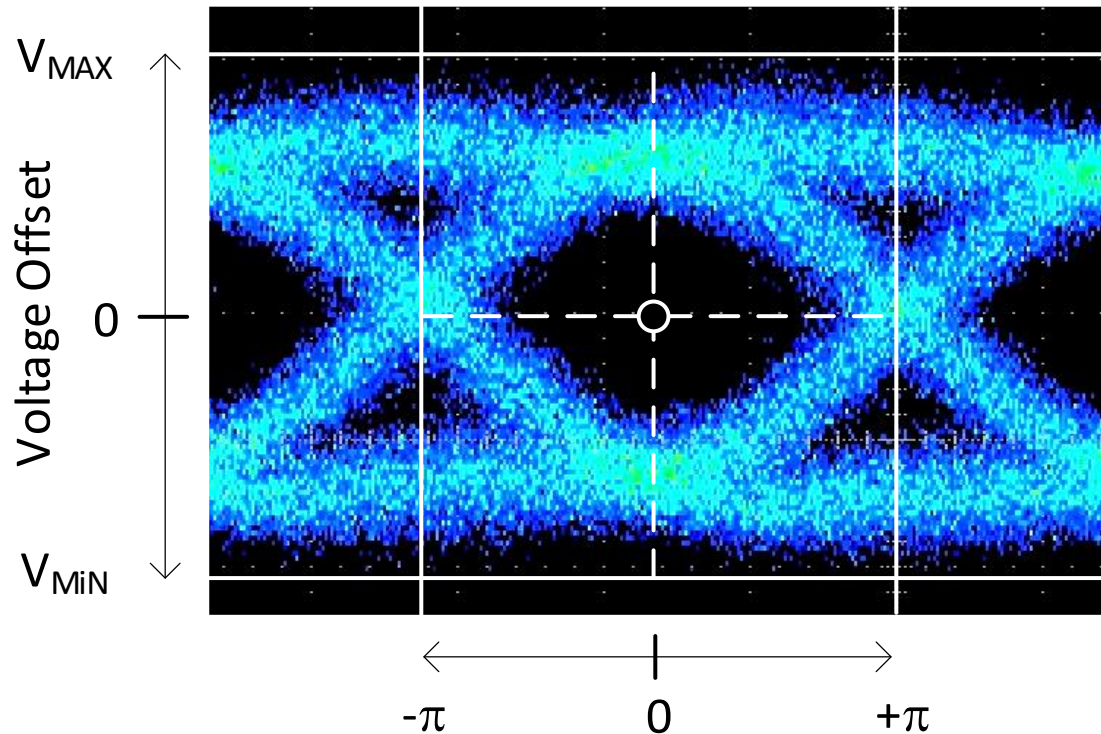
- Intentional Jitter: How Jitter can help
- Summary
- References

Why Jitter Monitoring?



- ❑ Simulated/measured jitter budget for a 25Gb/s optical link [Takemoto JSSC 2014]
- ❑ Jitter difficult to predict and mitigate at simulation time

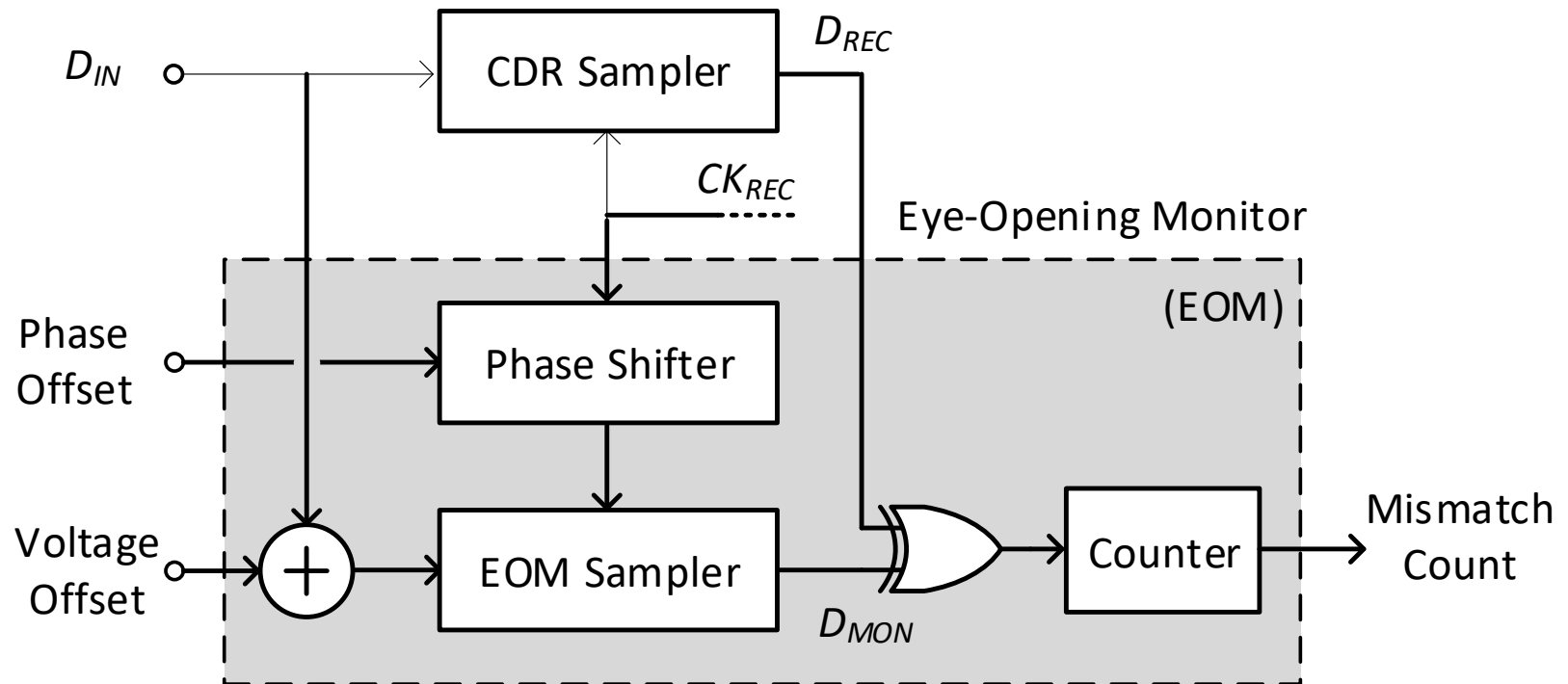
Ideal Sampling Position



- ❑ Sample in the middle of horizontal eye opening
- ❑ Slice it with a level at the middle of vertical eye opening
- ❑ These are hard to predict at design time

Eye-Opening Monitor

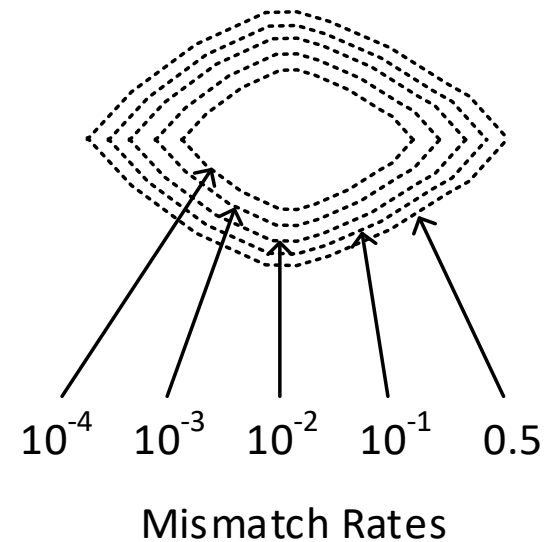
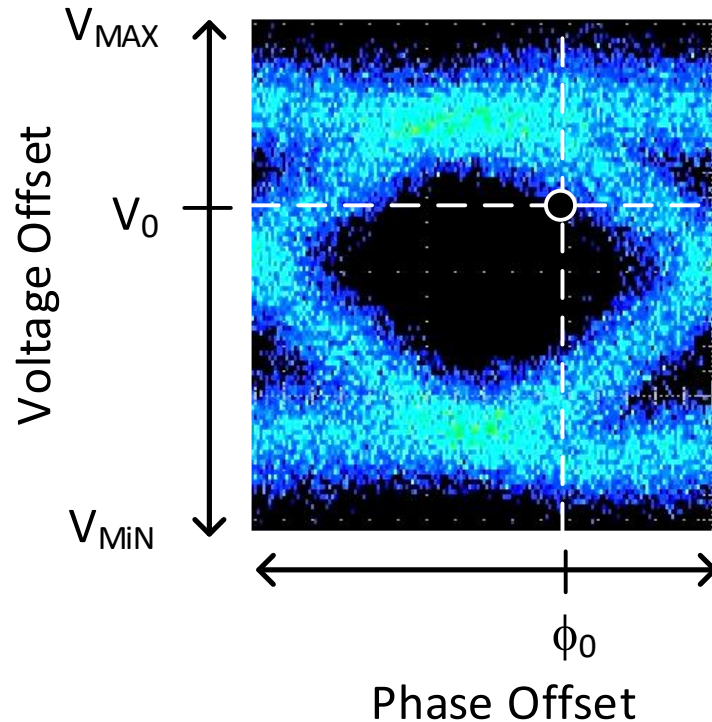
[Noguchi JSSC '08]



- ❑ EOM samples data at a phase/voltage offset away from CDR sampling point
- ❑ Comparing the two samples creates an “eye map”

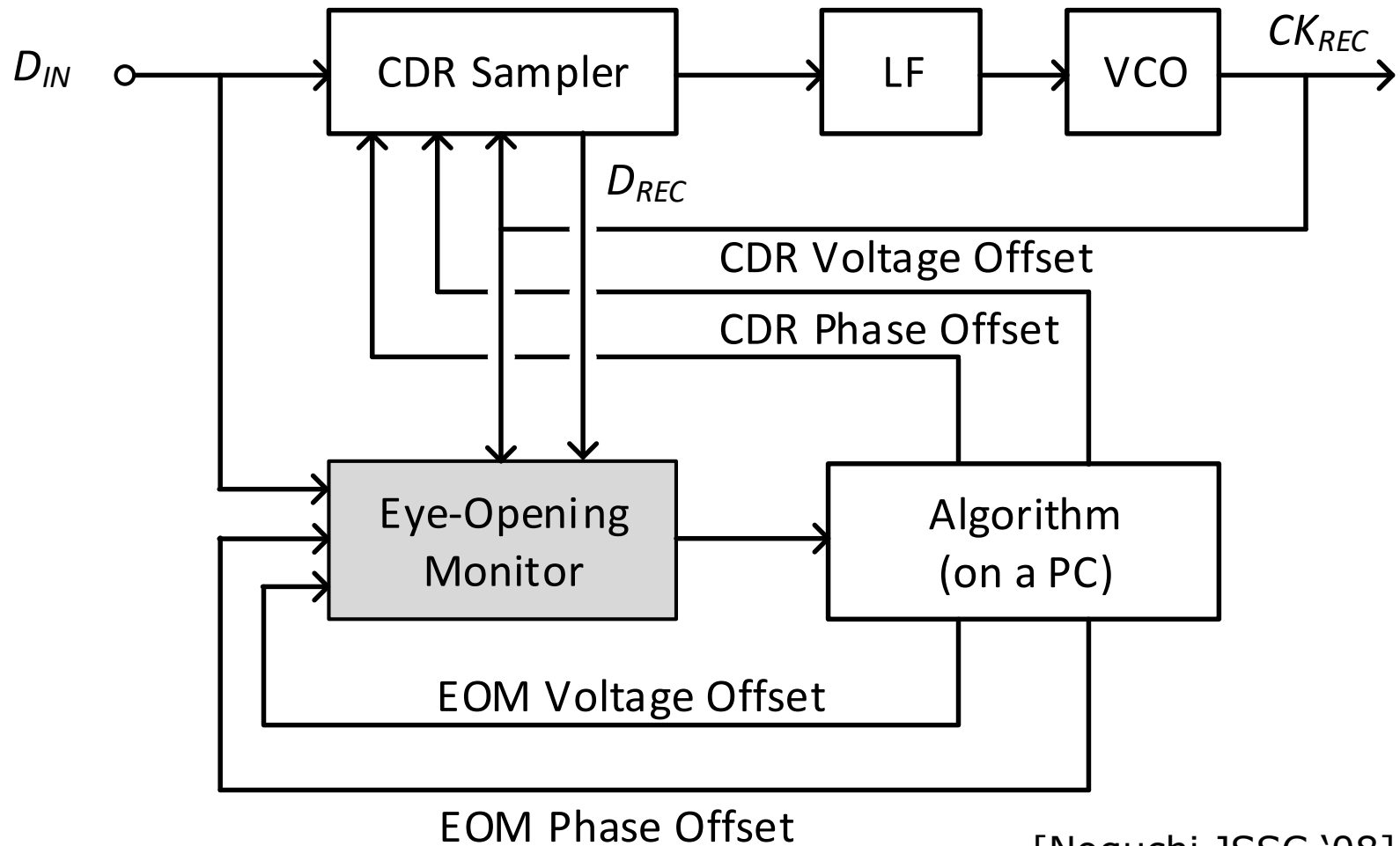
Search for Ideal Sampling Position

[Noguchi JSSC '08]



- ❑ Comparing CDR and EOM data creates eye contours
- ❑ Adaptive algorithms will position CDR sampling location

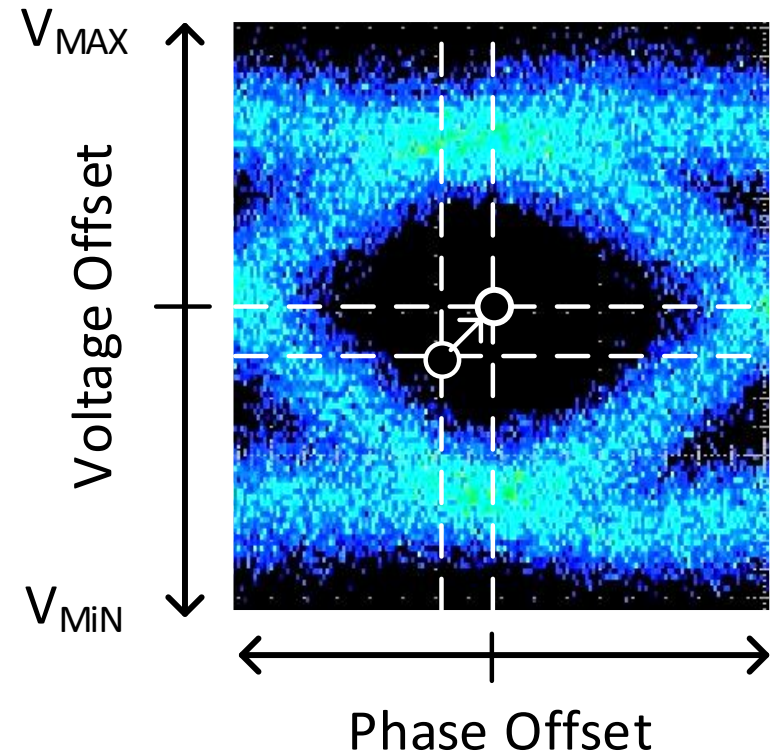
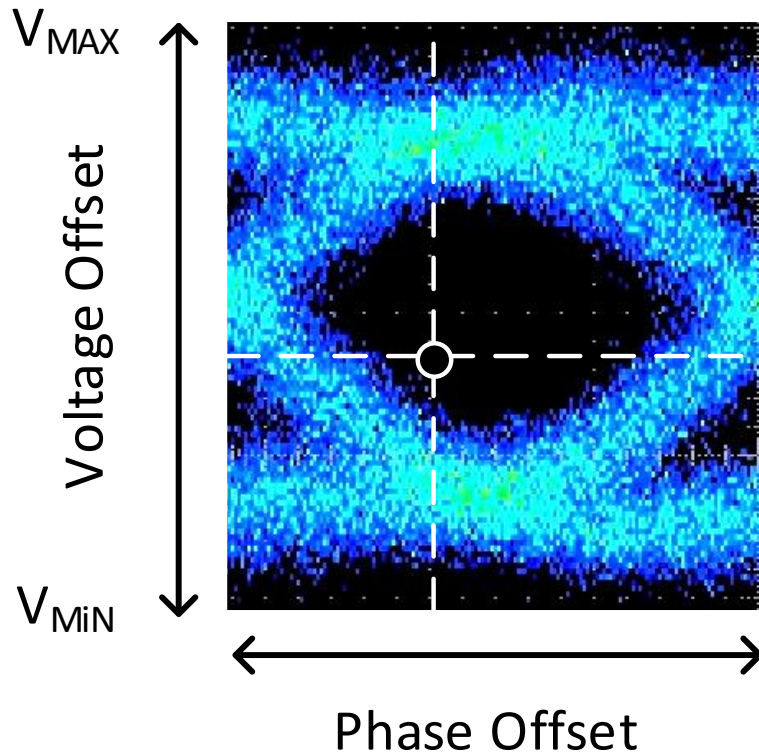
CDR with Eye-Opening Monitor



[Noguchi JSSC '08]

Moving to Ideal Position

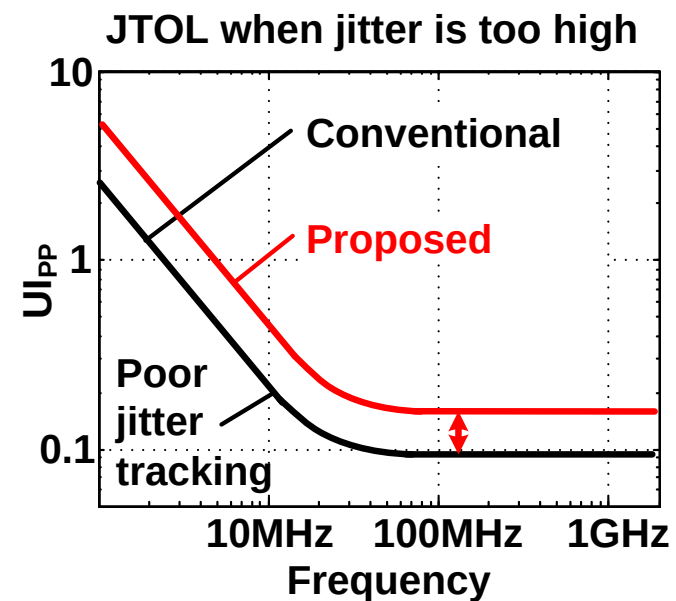
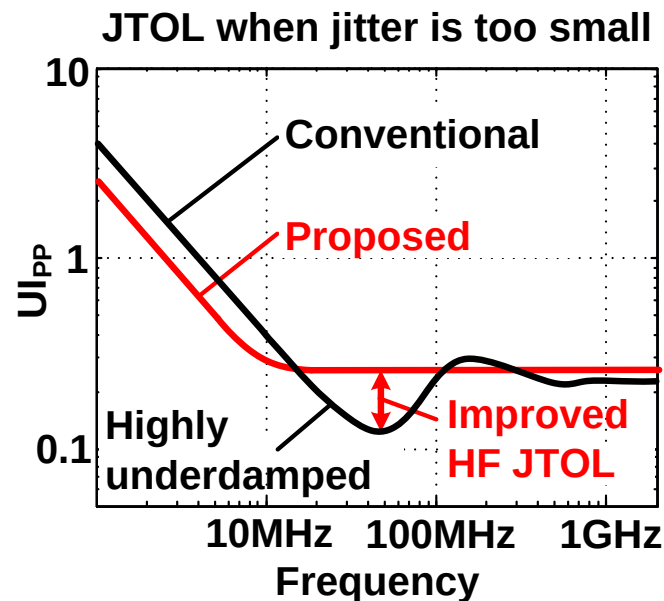
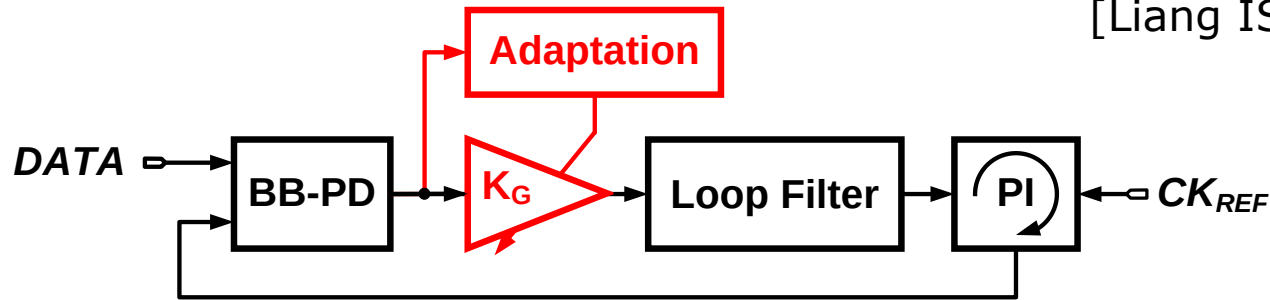
[Noguchi JSSC '08]



- Initial sampling position of CDR is detected using EOM
- Sampling position is moved to the center of the eye

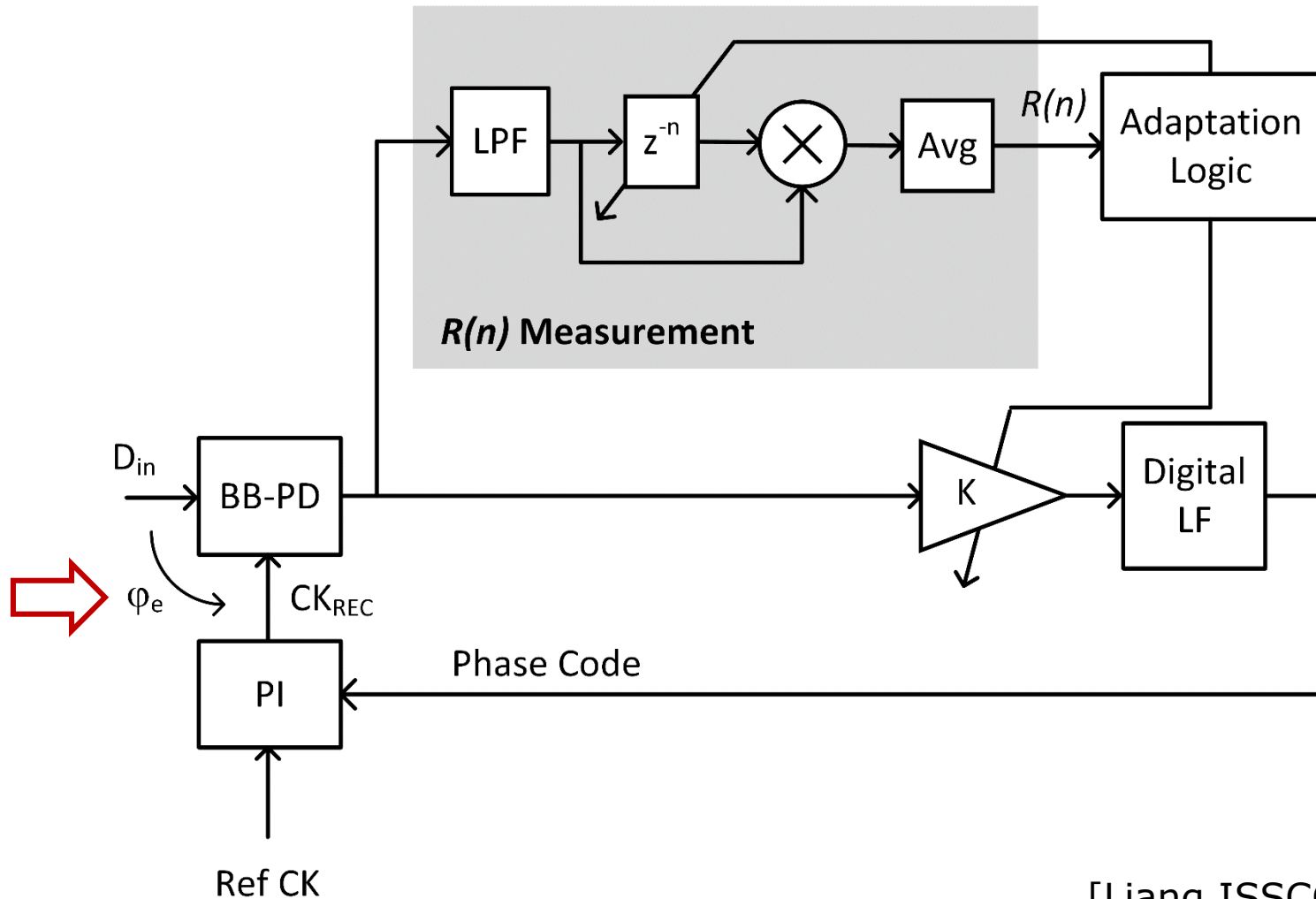
Jitter Monitoring for Jitter Tolerance

[Liang ISSCC'17]



□ Adapt loop gain (K_G) to maximize JTOL in PI-based CDR

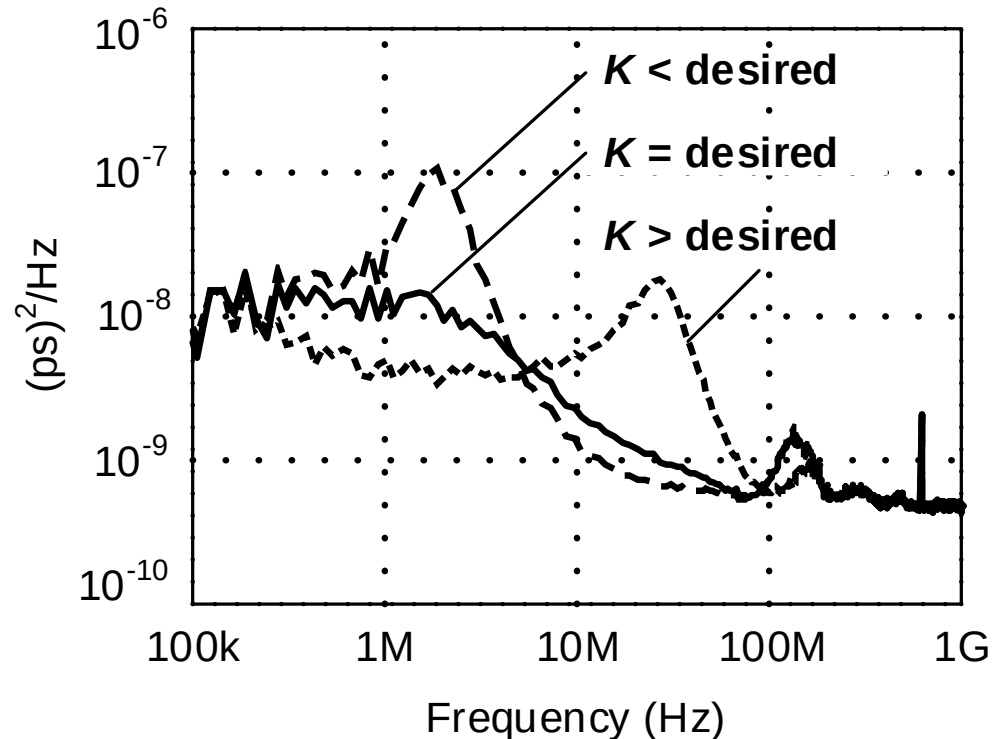
Monitoring Jitter at BB-PD Output



[Liang ISSCC'17]

PSD of Relative Jitter

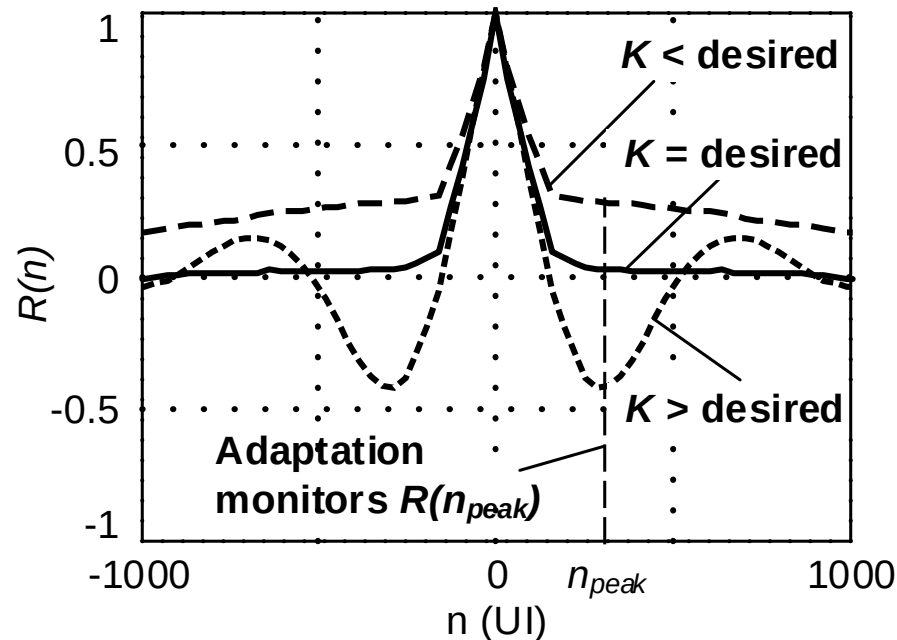
[Liang ISSCC'17]



- Power Spectral Density (PSD) versus loop gain (K)
 - The total power is in units of $(ps)^2$
 - Desired K corresponds to no overshoot or undershoot
 - Hard to measure

Measure Autocorrelation

[Liang ISSCC'17]

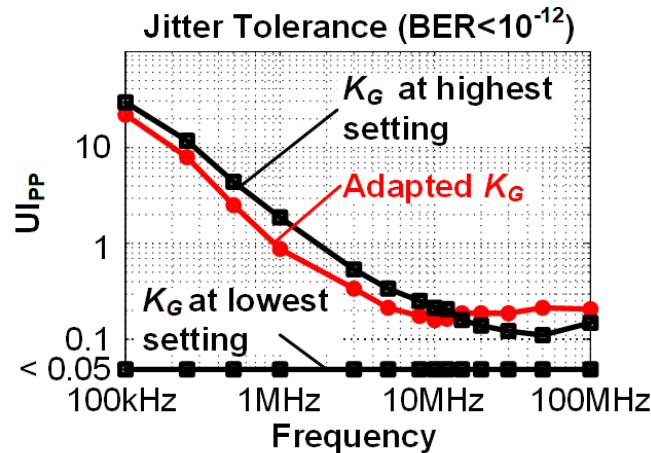


- Use autocorrelation of PD output, $R(n)$, instead
 - Reveals similar behavior as PSD
 - Adjust K to arrive at “critically damped” condition
 - How? Start with max K , measure n_{peak}
 - Reduce K gradually to force $R(n_{peak})$ to zero.

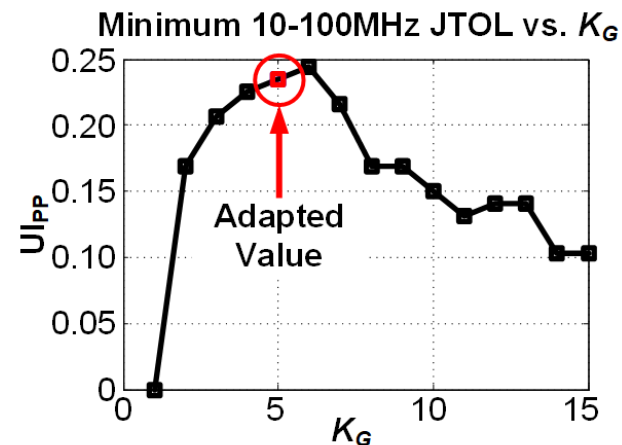
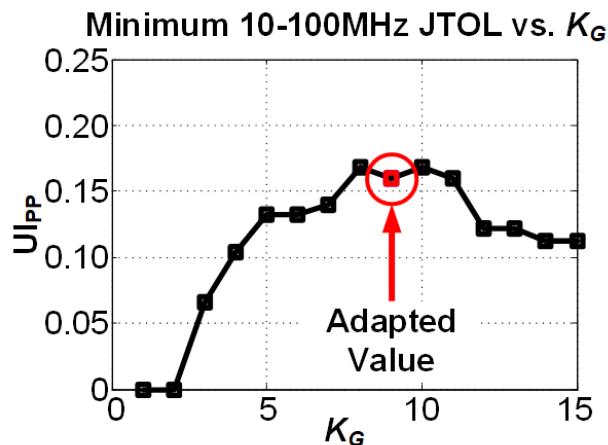
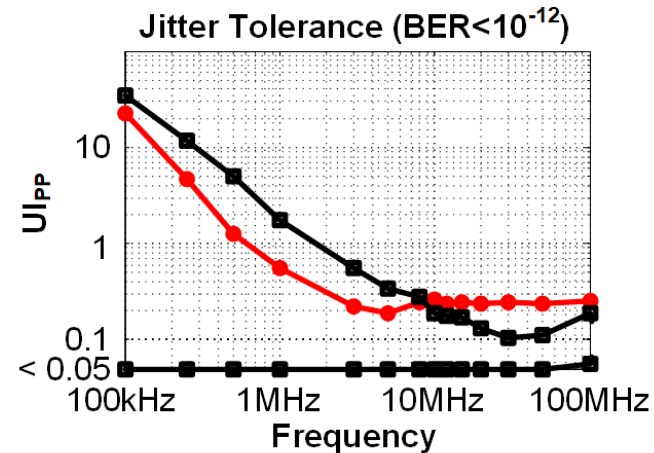
Measured Jitter Tolerance

[Liang ISSCC'17]

Test Case 1

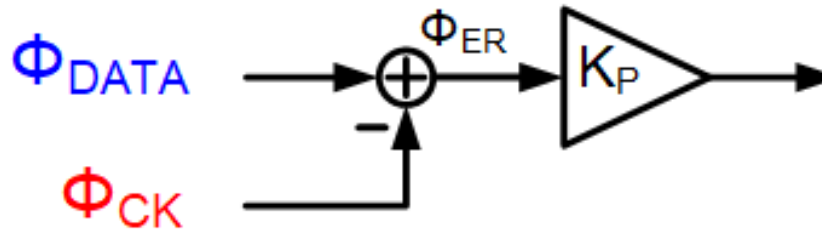


Test Case 2



Measuring Absolute Jitter

[Liang JSSC '15]



$$K_P \cdot \Phi_{ER} = K_P \cdot (\Phi_{DATA} - \Phi_{CK})$$

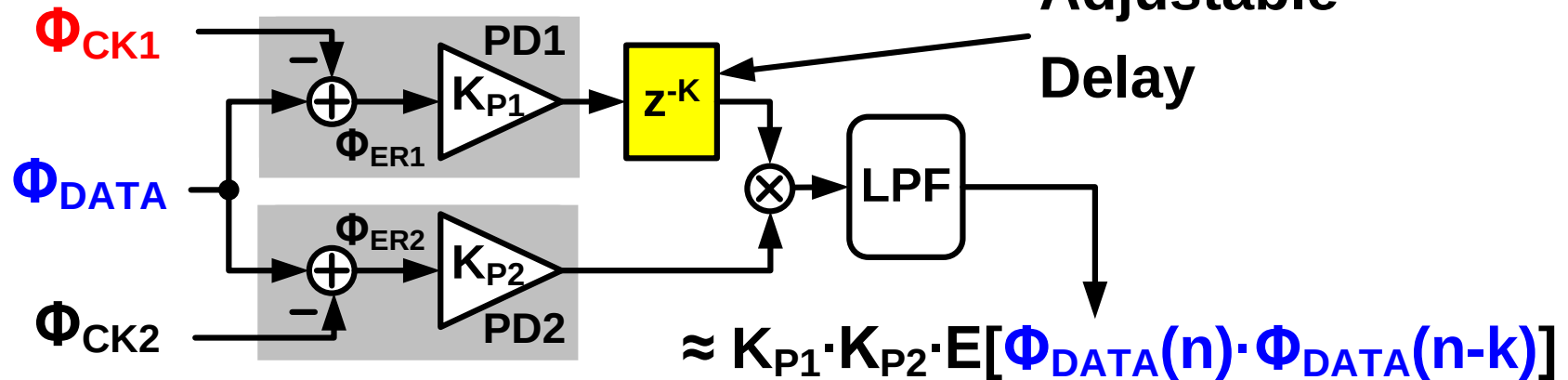
- ❑ Interested in distinguishing between jitter in the incoming data and the recovered clock
- ❑ Only the relative jitter between the two is observable
- ❑ Without ideal clock, how to measure absolute jitter

Use Two Phase Detectors

[Liang JSSC '15]

Adjustable

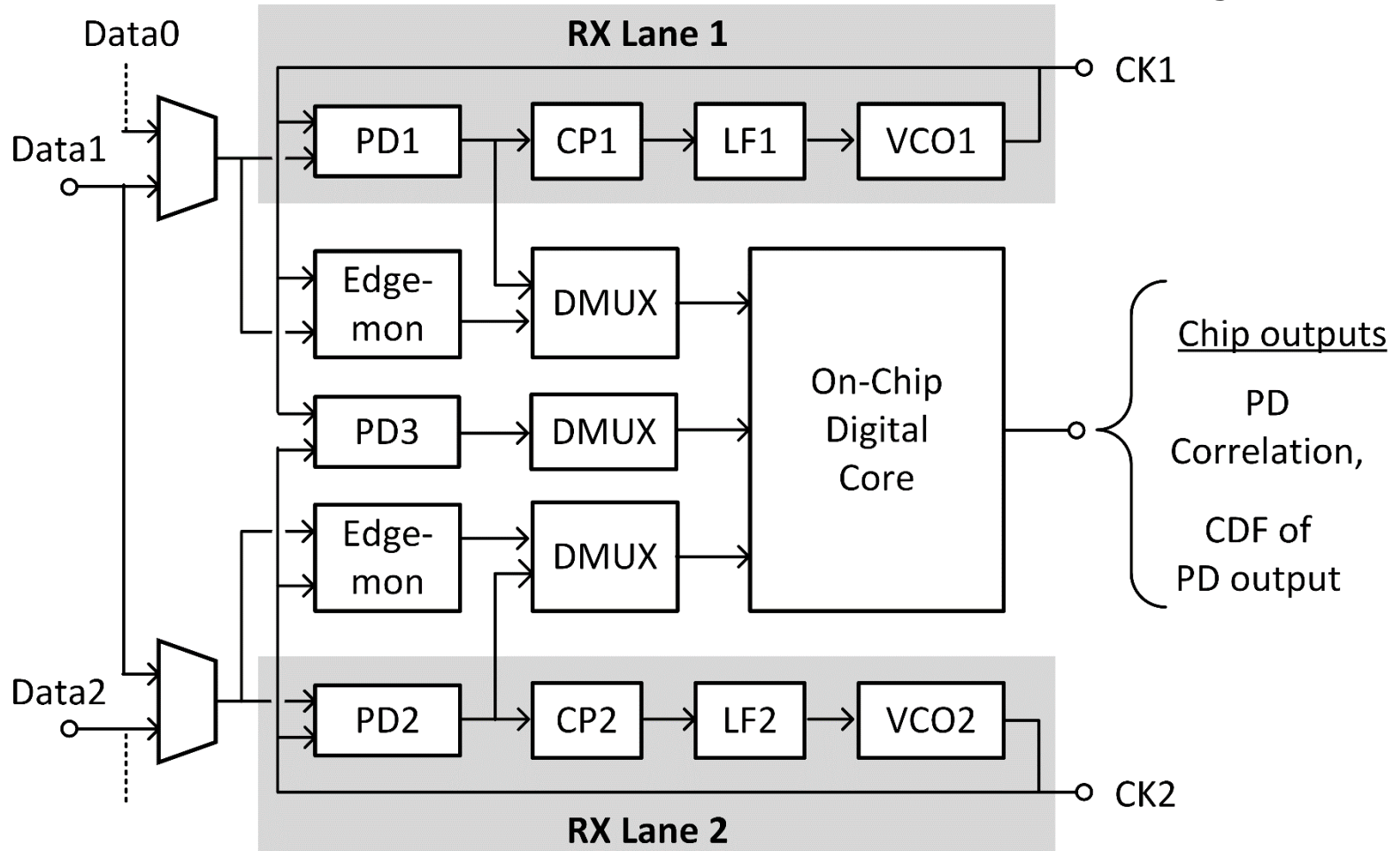
Delay



- ❑ Assumes Φ_{CK1} and Φ_{CK2} are uncorrelated
- ❑ Insert adjustable delay on one side
- ❑ Combine the two for autocorrelation function $R_{DATA}(k)$
- ❑ If jitter is stationary
- ❑ $E[\Phi_{DATA}(n) \cdot \Phi_{DATA}(n-k)] = R_{DATA}(k)$
- ❑ LPF approximates the Expected Value
- ❑ Fourier Transform of $R_{DATA}(k)$ gives the PSD of Φ_{DATA}

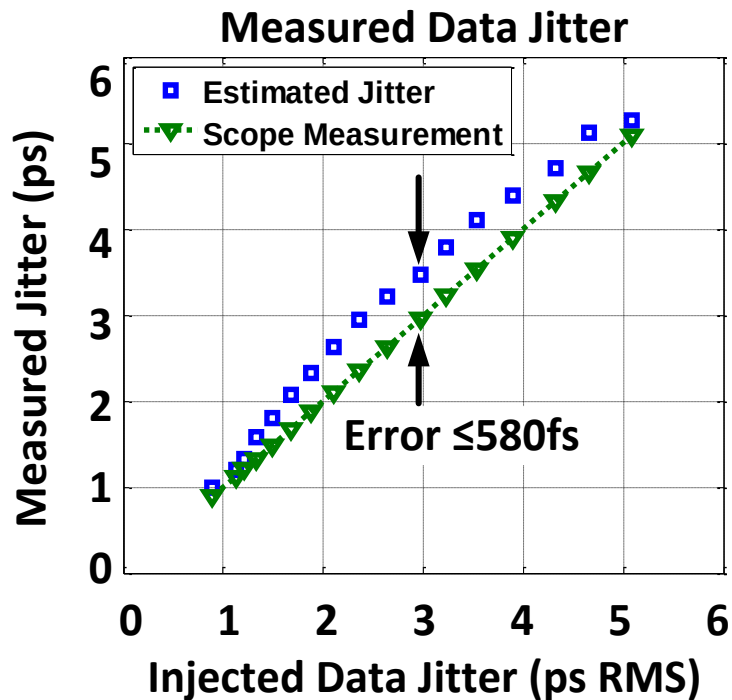
Implementation in Multi-Lane CDR

[Liang JSSC '15]

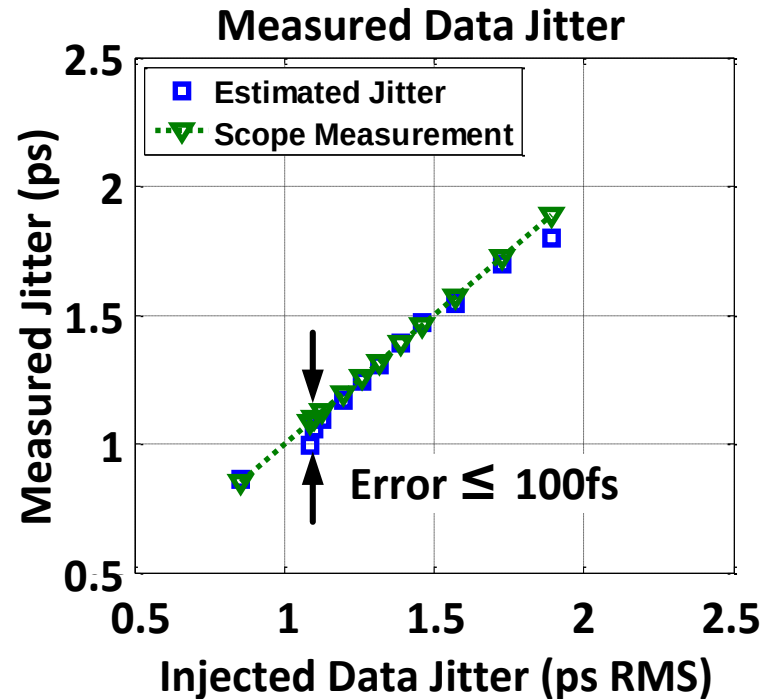


Measured Results [Liang JSSC'15]

100MHz SJ Applied



20-100MHz RJ Applied



Estimated Jitter

Measurement from 80GS/s real-time scope

Outline

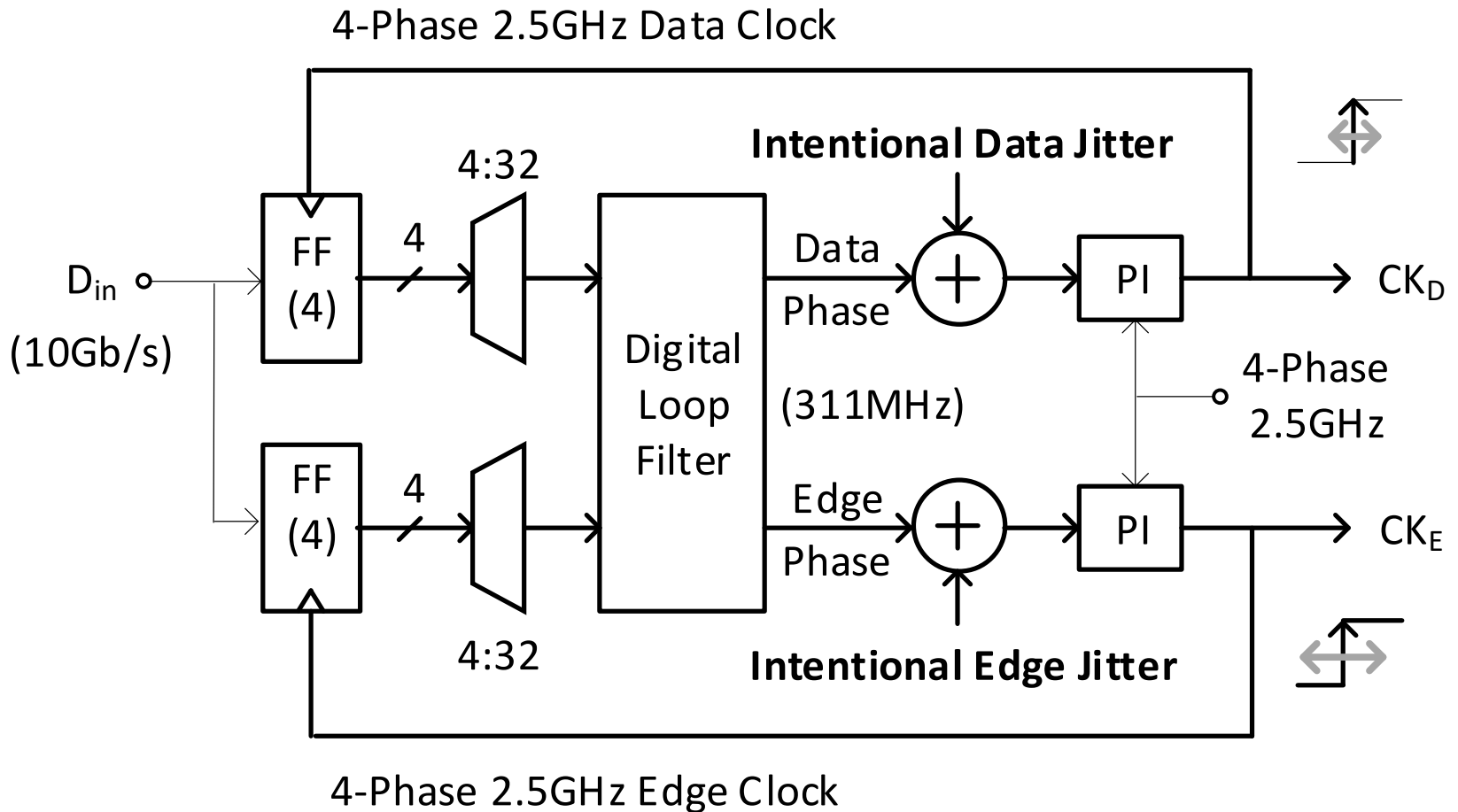
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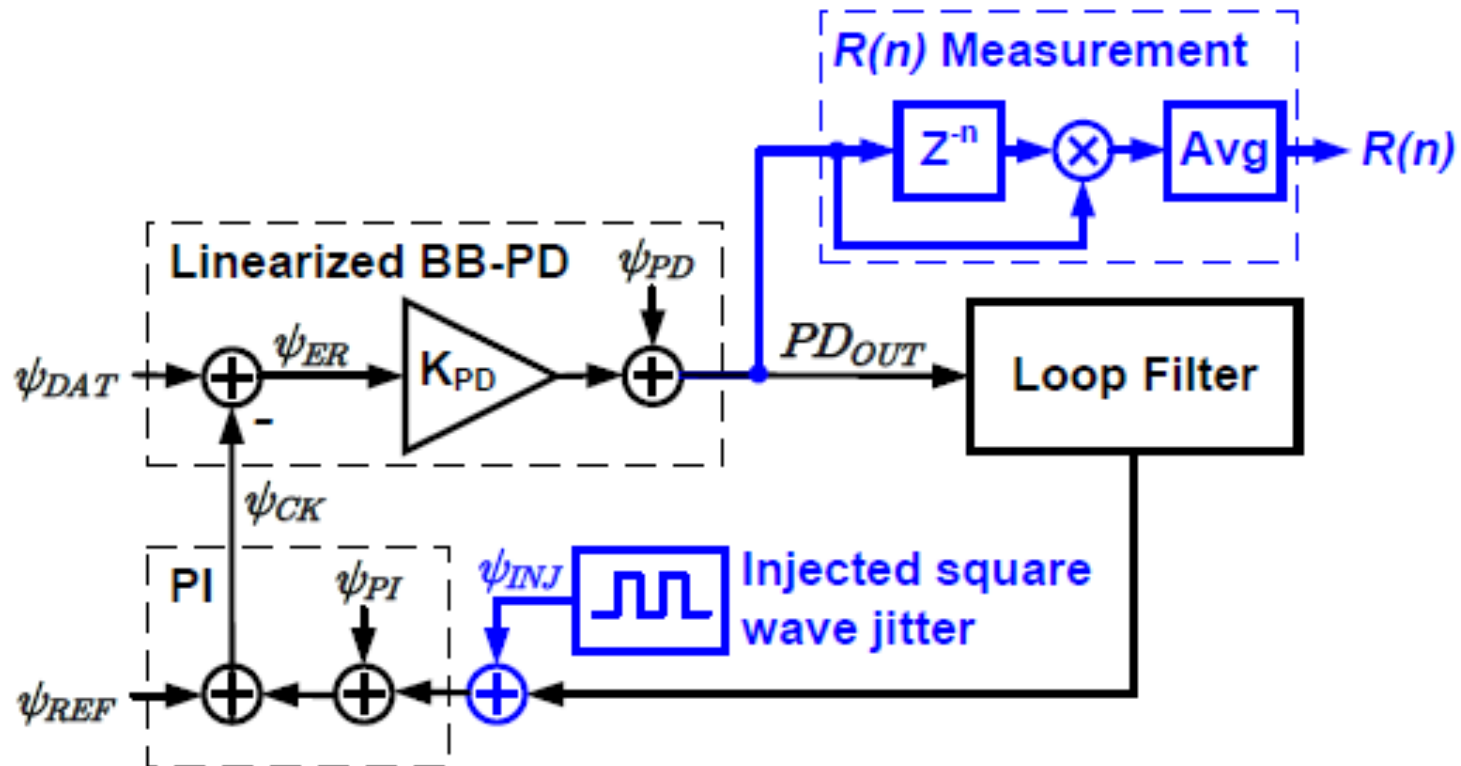
Intentional Jitter to Improve Linearity

[Takauchi JSSC '03]



Jitter Injection for Measurement

[Liang CICC'17]

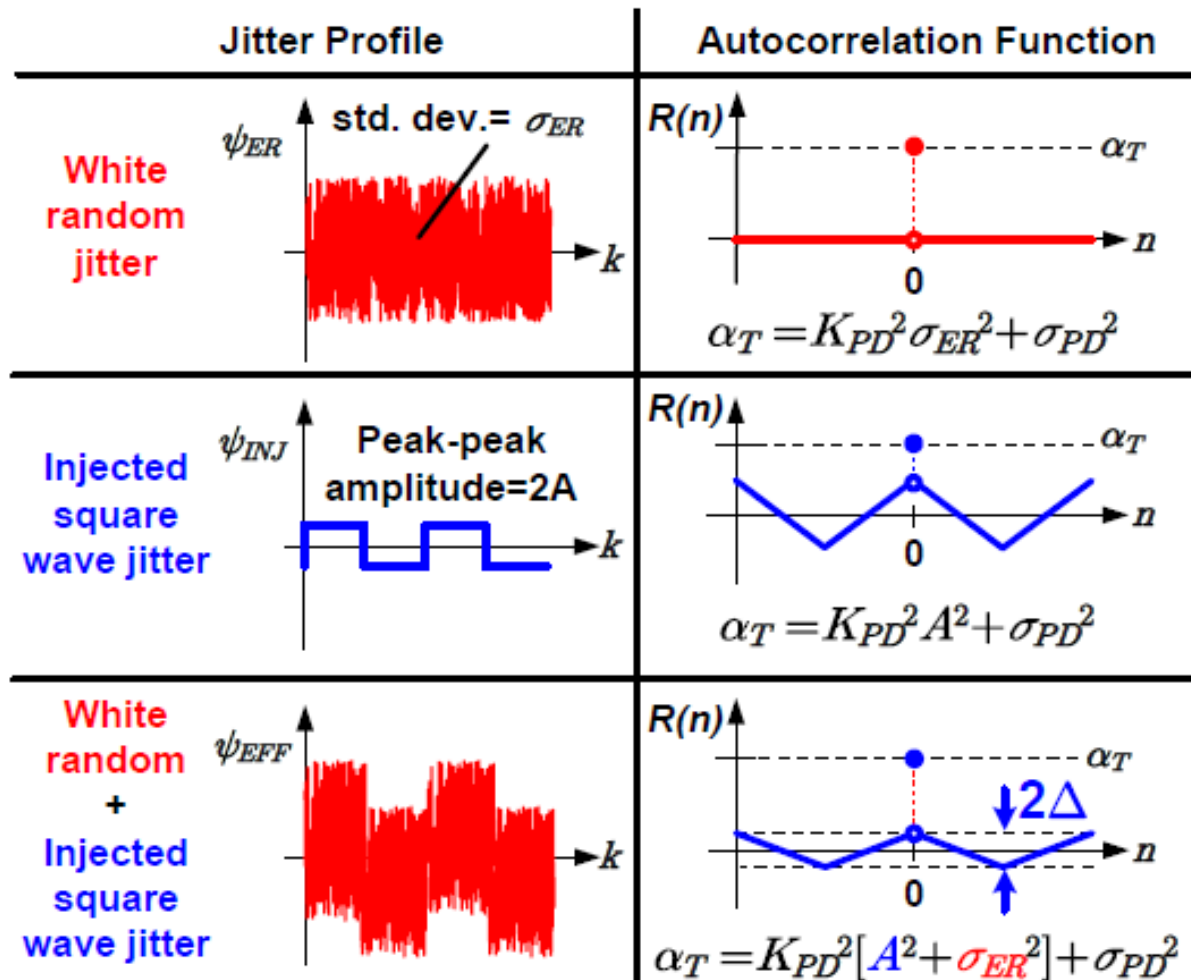


- Intentional jitter toggles LSB for PI of Edge CK
 - Helps calibrate BB-PD effective gain measurement
 - Improves accuracy of relative jitter measurement

Injected Jitter Provides Observability

[Liang CICC'17]

*Outstanding Student Paper Award from CICC2017!



Other Relevant Topics

- Effect of Jitter on Data Converters
 - Both DAC and ADC
 - Time-Interleaved ADC's
- Effects of Jitter on $\Delta\Sigma$ ADC's
 - Jitter noise is shaped by the NTF
- Effects of Jitter on Wireless Systems/Circuits
- Jitter Amplifications by Passive Channel

Summary

- Jitter definitions:
 - Absolute jitter: deviation from an ideal clock timing
 - Relative jitter: timing difference between two real clocks
 - Period jitter: deviation in period from average period

- Jitter histogram, PDF, PSD
 - Histogram/PDF provide statistics: mean, rms, peak-to-peak
 - PSD is based on jitter behavior over time (autocorrelation)
 - PSD provides information in frequency domain

- Jitter monitoring unavoidable as we move to higher rate
 - Monitoring is the first step towards jitter mitigation

- Jitter is injected intentionally to improve observability

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- N. Da Dalt and A. Sheikholeslami, "Understanding Jitter and Phase Noise - A Circuits and Systems Perspective" by Cambridge University Press, 2018

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- J. Lee et al., "Analysis and Modeling of Bang-Bang Clock and Data Recovery Circuits," JSSC, pp. 1571-2004, Sep. 2004

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- H. Noguchi, et al., "A 40-Gb/s CDR Circuit with Adaptive Decision-Point Control Based on Eye-Opening Monitor Feedback," JSSC, vol. 43, no. 12, pp. 2929-2938, Dec 2008

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- J. Liang, et al., "A 28Gb/s Digital CDR with Adaptive Loop Gain for Optimum Jitter Tolerance," ISSCC, pp. 122-123, Feb 2017
- J. Liang, et al., "On-Chip Measurement of Clock and Data Jitter With Sub-Picosecond Accuracy for 10 Gb/s Multilane CDRs," JSSC, vol. 50, no. 4, pp. 845-855, Apr. 2015

Intentional Jitter

- H. Takauchi et al., "A CMOS Multichannel 10-Gb/s Transceiver," ISSCC 2003, paper 4.2. Expanded version in JSSC, pp. 2094-2100, Dec. 2003
- J. Liang, et al., "Jitter Injection for On-Chip Jitter Measurement in PI-Based CDRs," CICC, pp. 1-4, Apr. 2017

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