Clock and Data Recovery Architectures & Circuits

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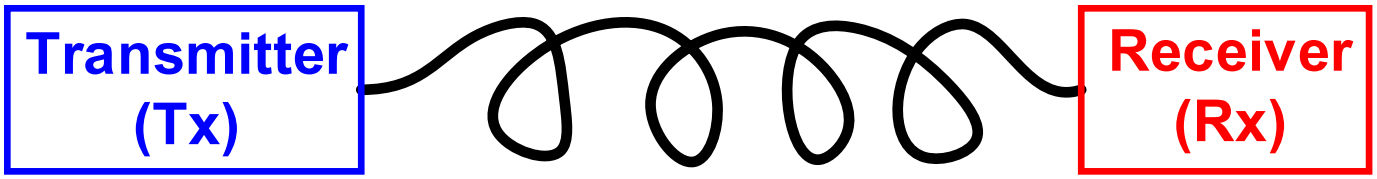
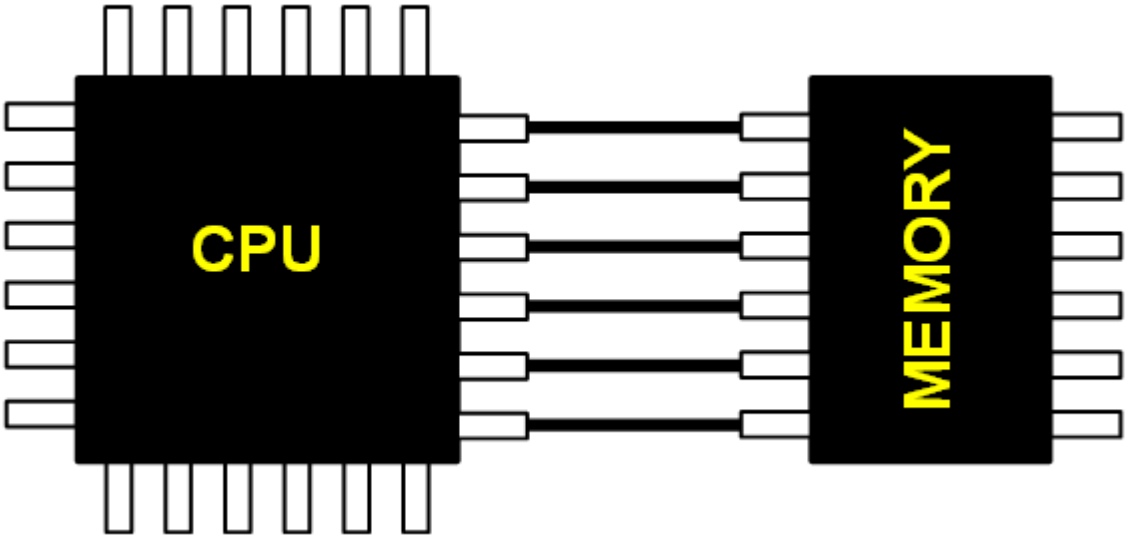
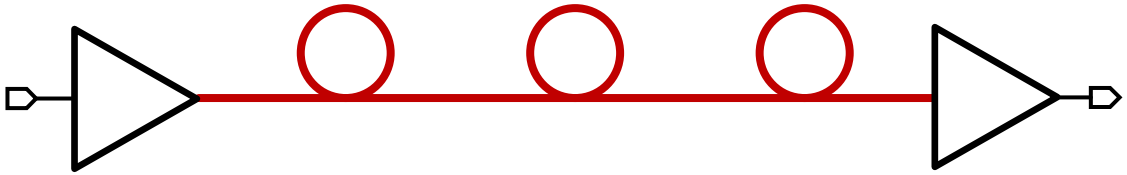
Serial Link Applications



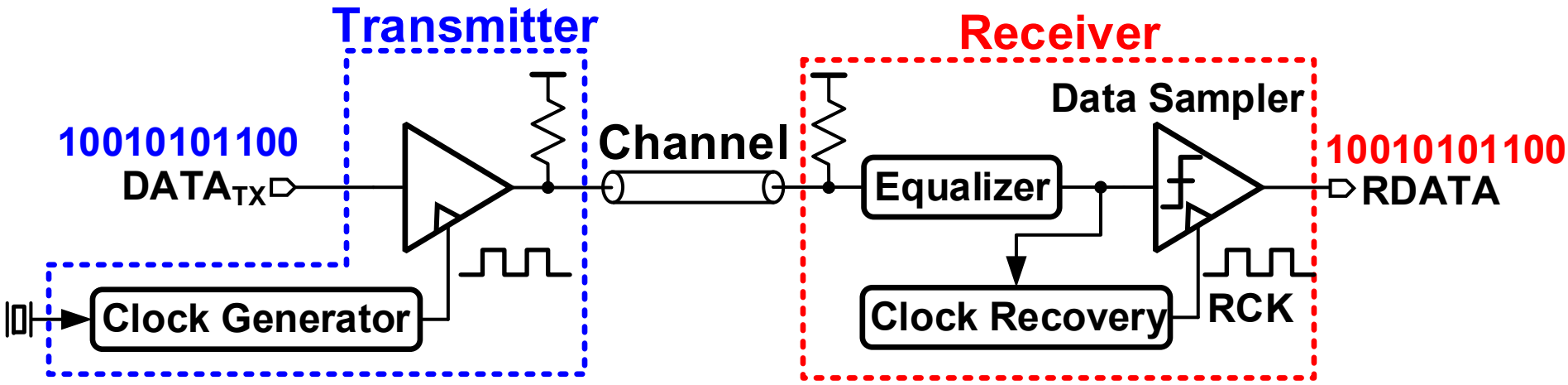
Chip-to-chip Electrical link



Optical link



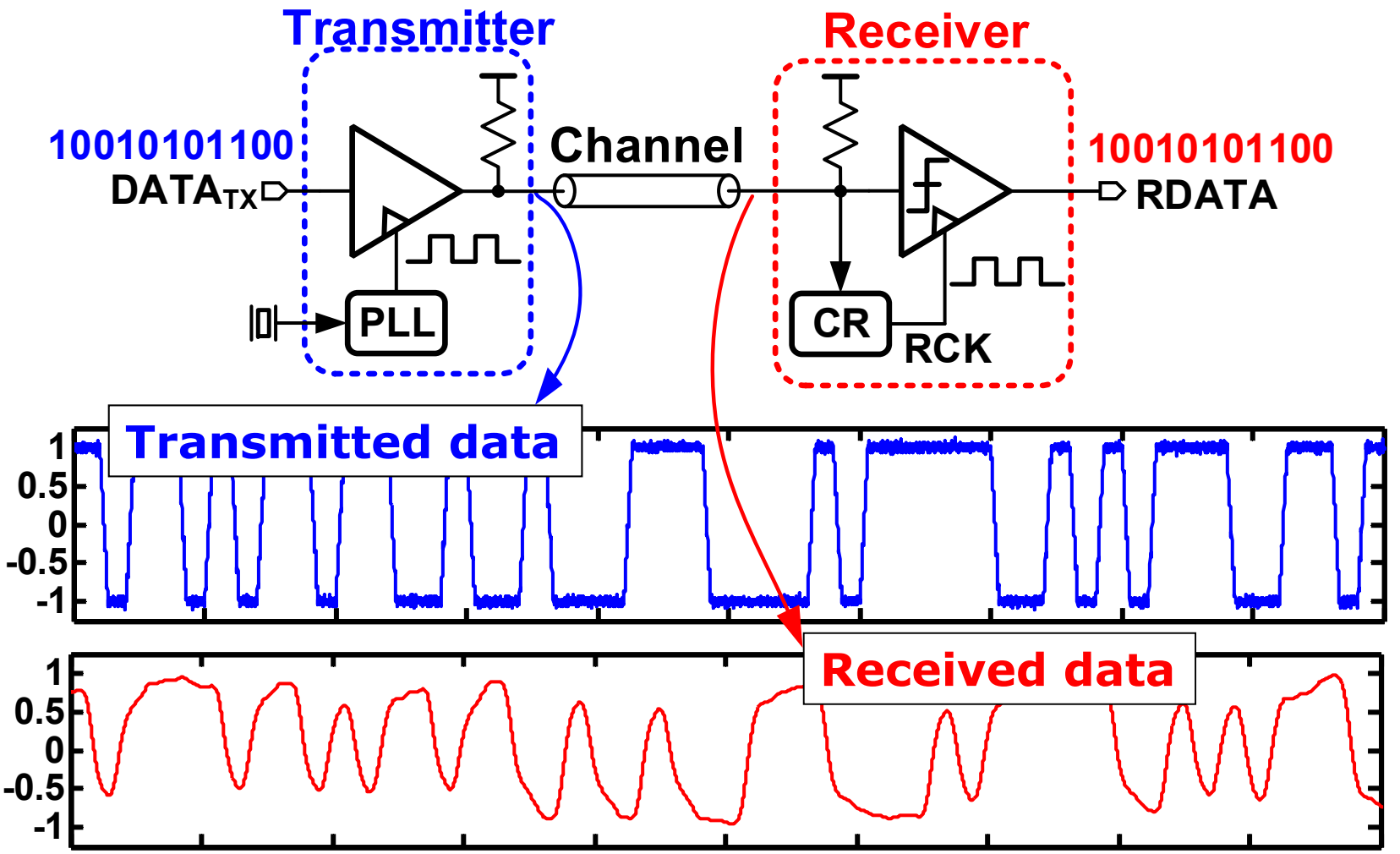
Serial Link Components



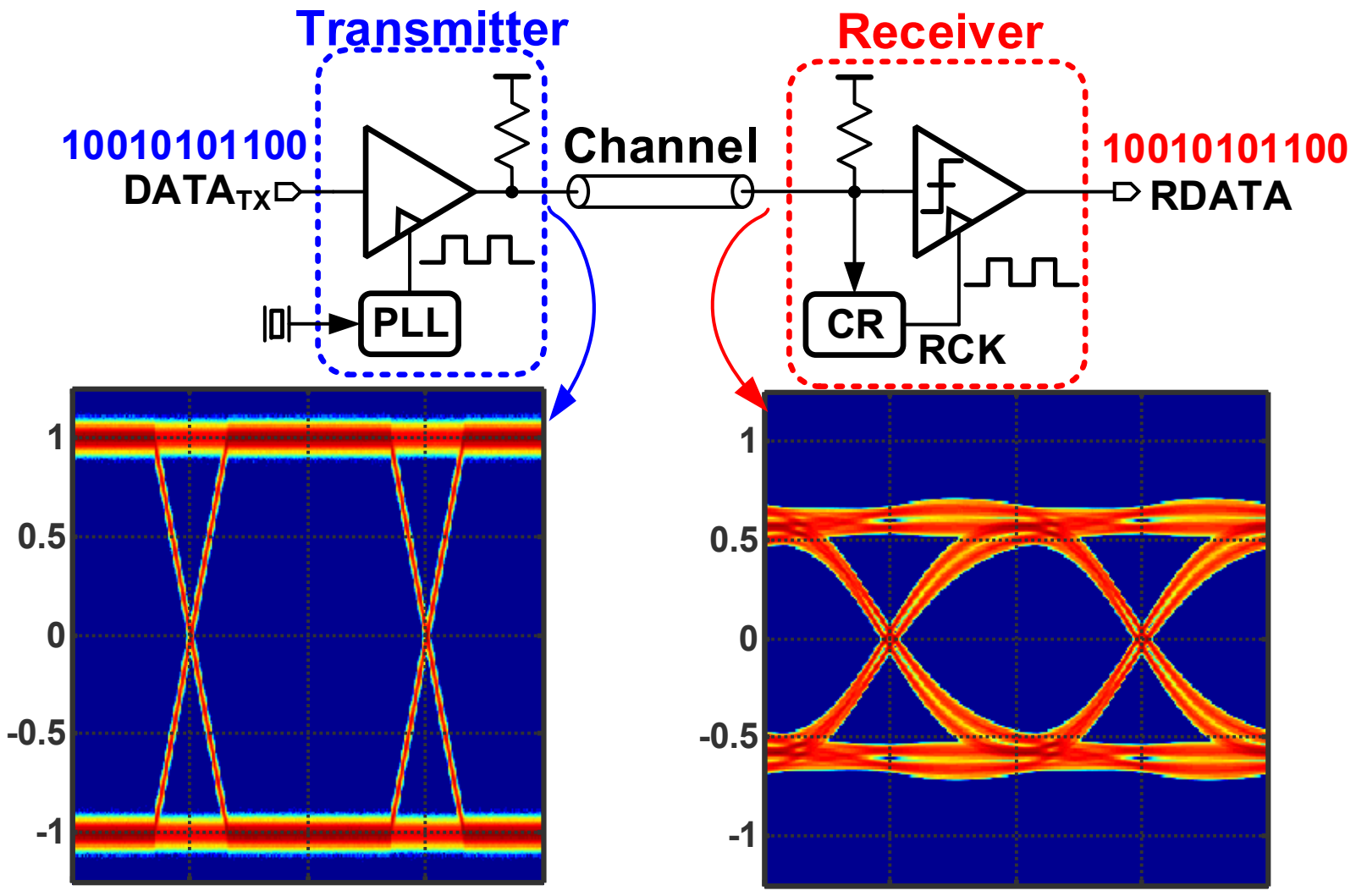
- Transmitter
- Channel
- Receiver

- Clock Recovery (CR) + Data sampler = CDR

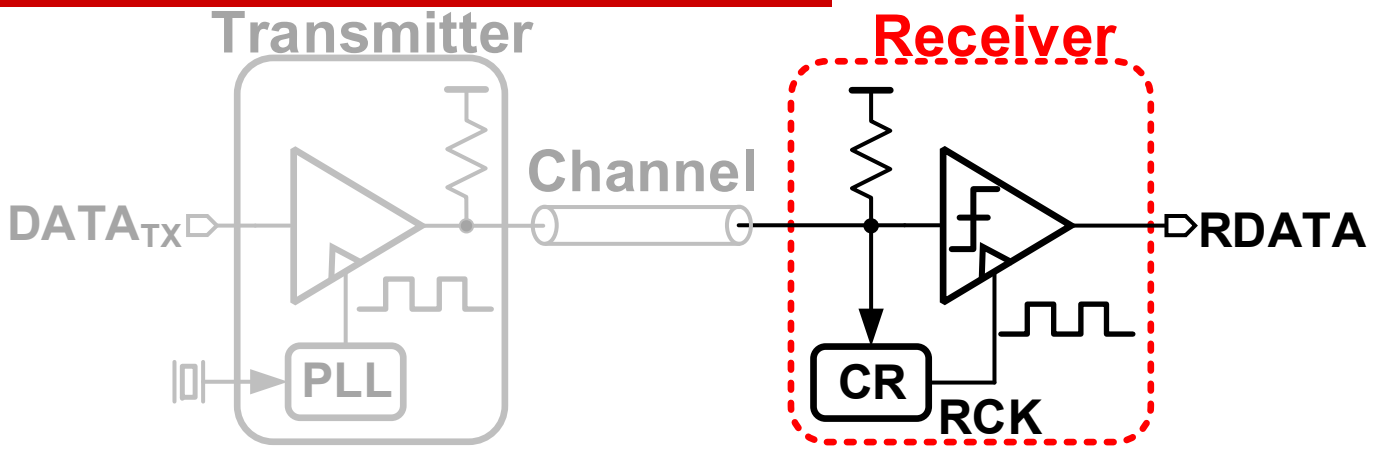
Serial Link Waveforms

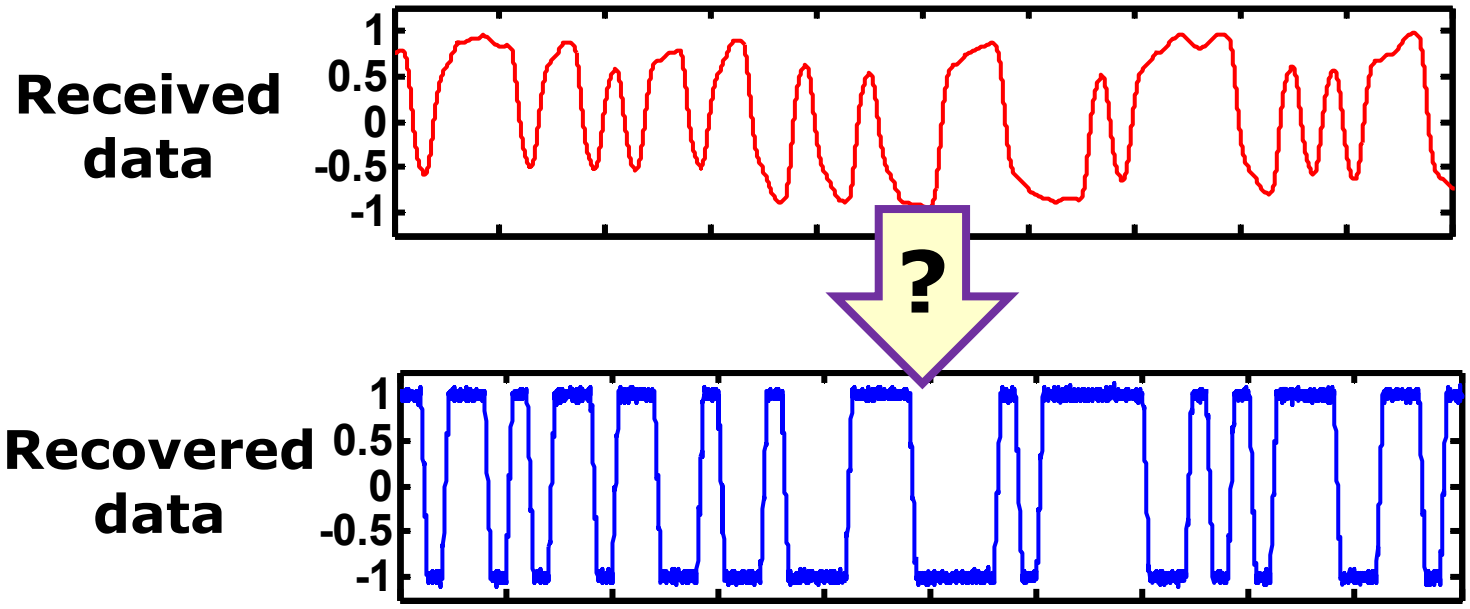


Serial Link Eye Diagrams



This Tutorial Focus: CDR

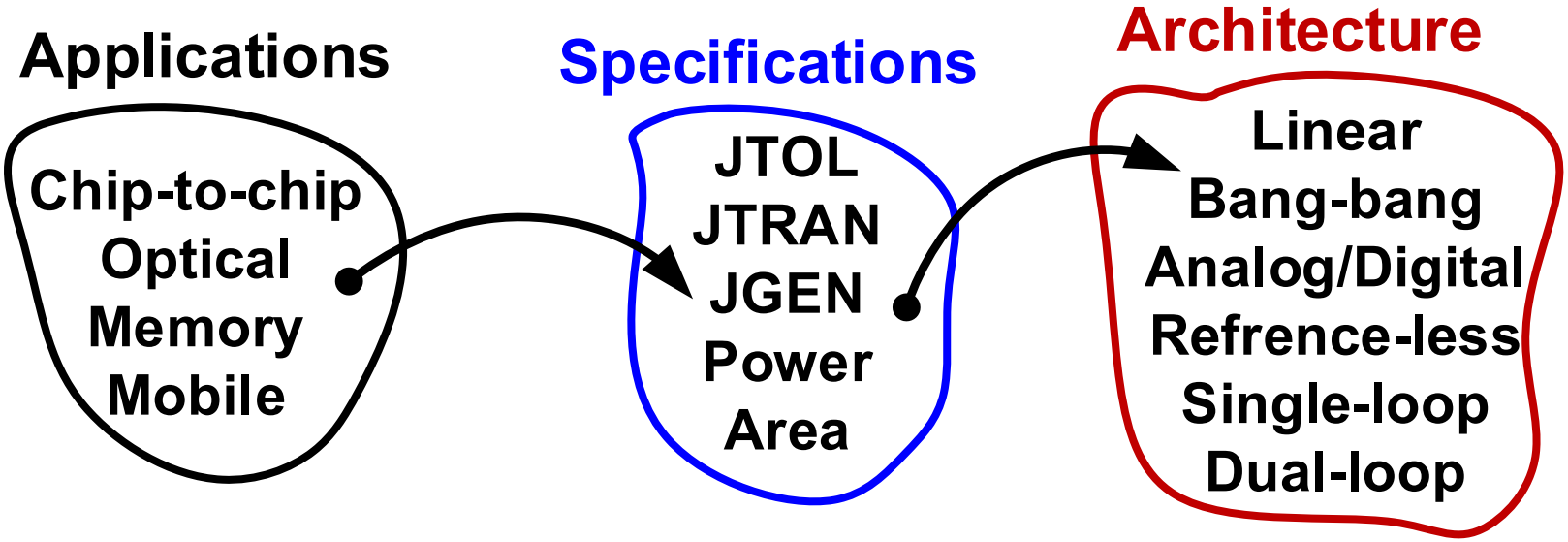




1. clock recovery

2. use the CDR to sample the data stream

Tutorial Goals



- Map application requirements to CDR specifications
- Optimal architecture choice based on CDR specs.
  - Exposure to different CDR architectures
  - Develop intuition for design tradeoffs
  - Awareness to practical considerations

Tutorial Roadmap

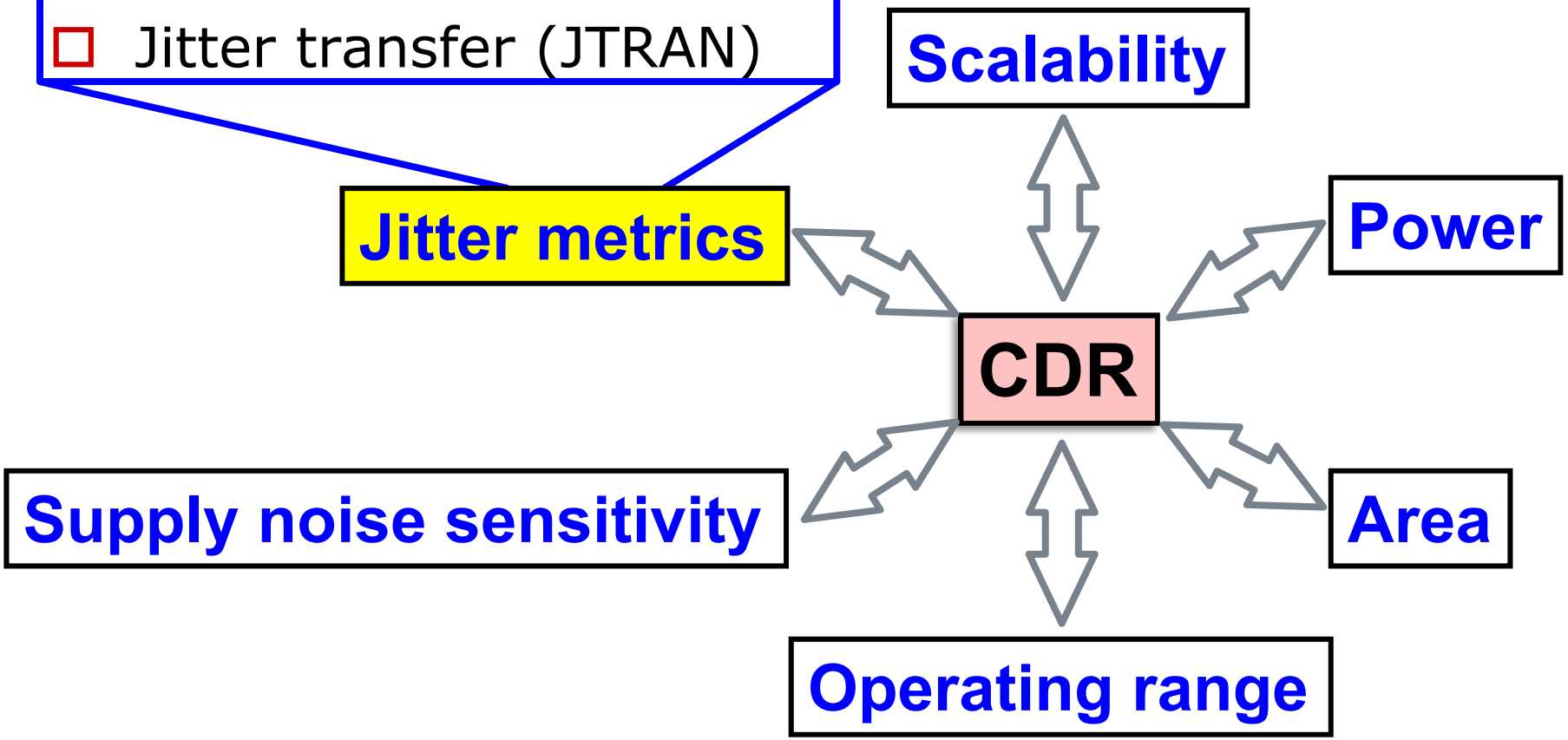
- Performance metrics

unique to CDR

- Basic architectures
  - Linear/Bang-bang
  - Digital
  - Hybrid
- Application-specific CDRs
  - Multi-lane chip-to-chip links
  - Repeaters for optical links and active cables
- Summary

CDR Performance Metrics

- Jitter tolerance (JTOL)
- Jitter generation (JGEN)
- Jitter transfer (JTRAN)

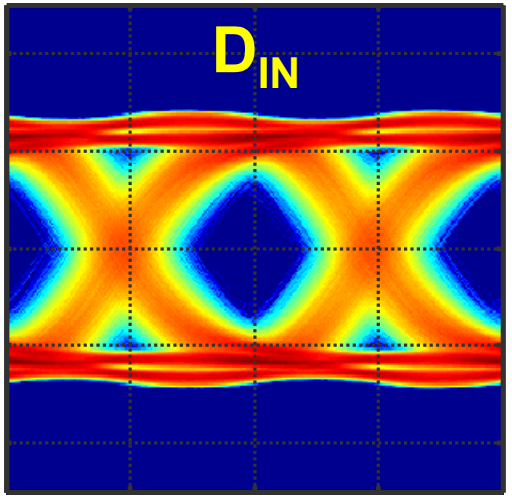


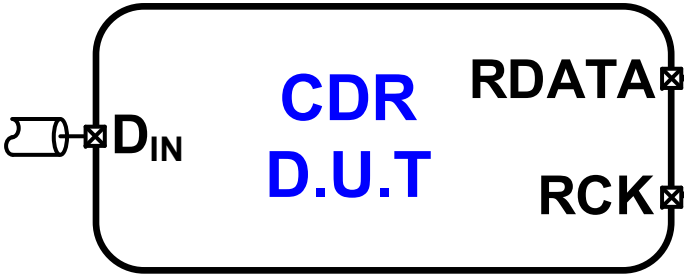
Jitter Tolerance (JTOL)

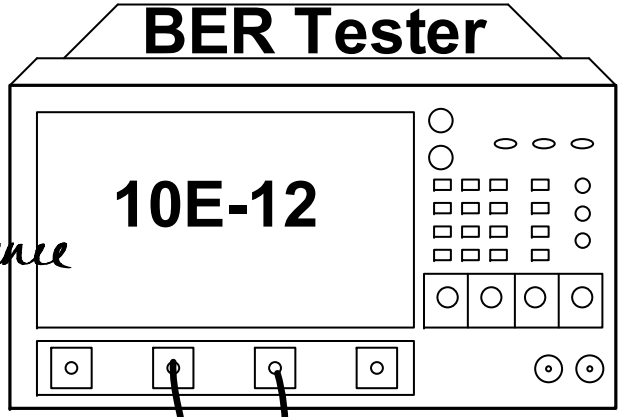
- Maximum tolerable input jitter for a given BER

$$\text{BER} = \frac{\text{Number of bit errors}}{\text{Number of transmitted bits}}$$

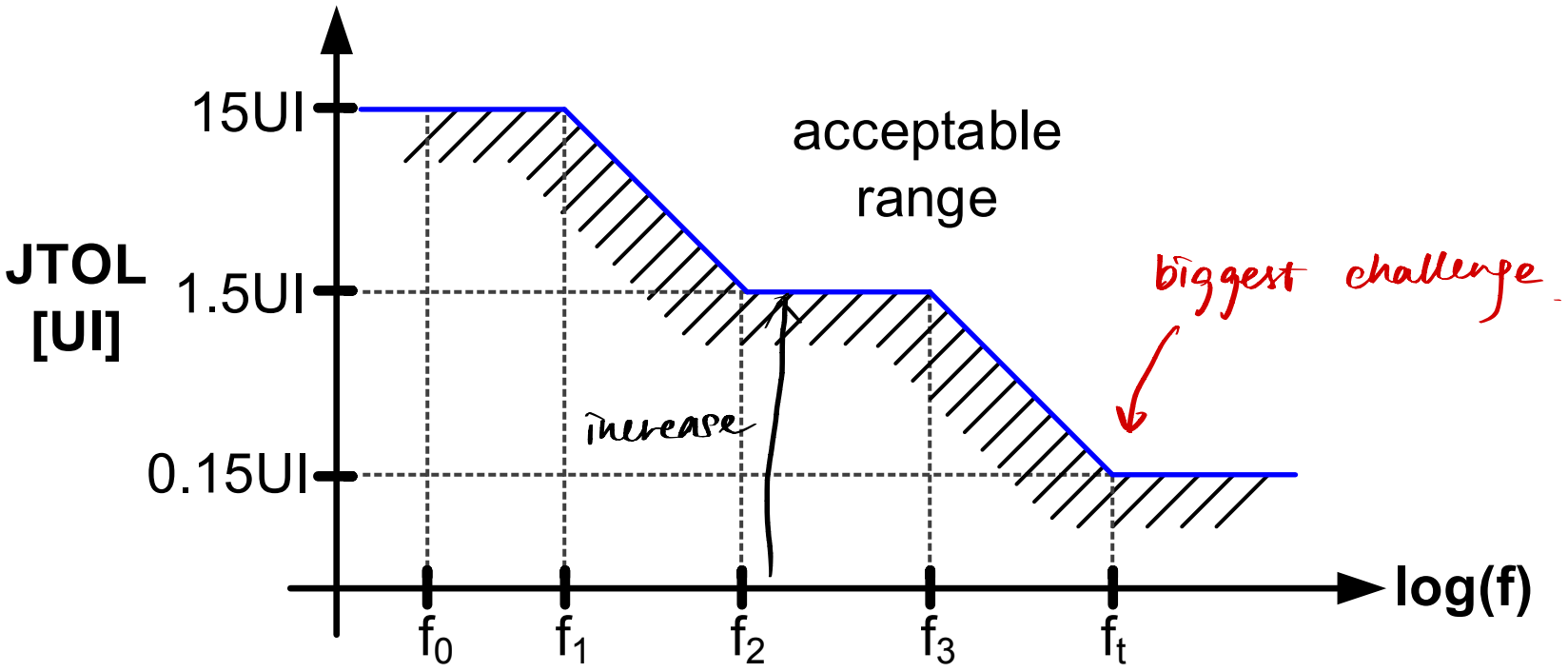
send 3×10^{12}, no error, 95% confidance







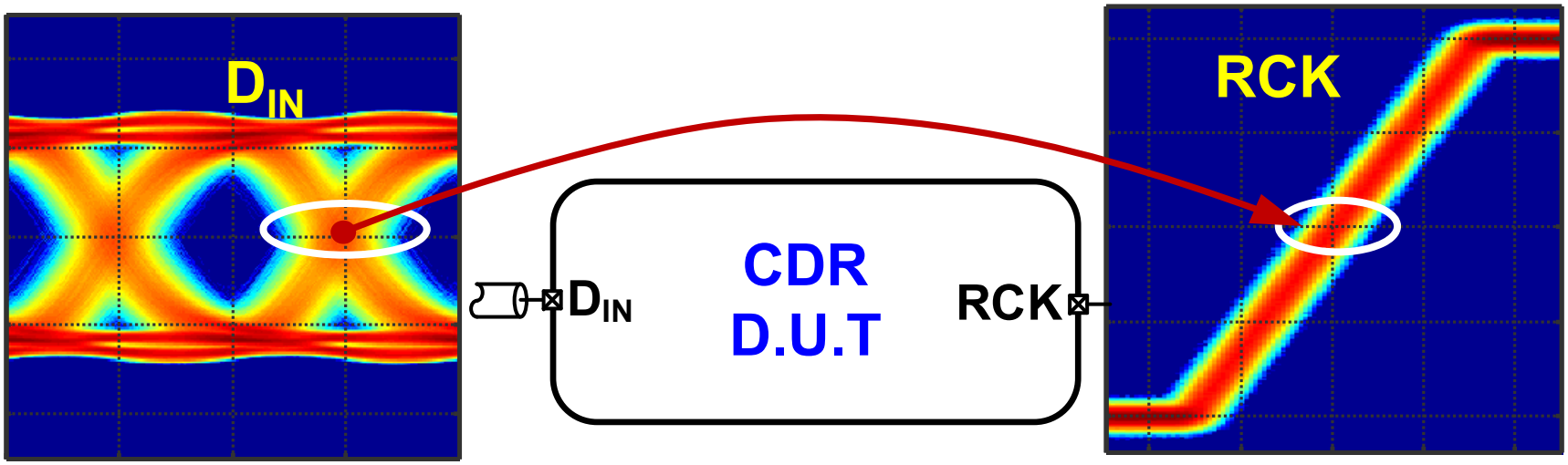
JTOL Mask



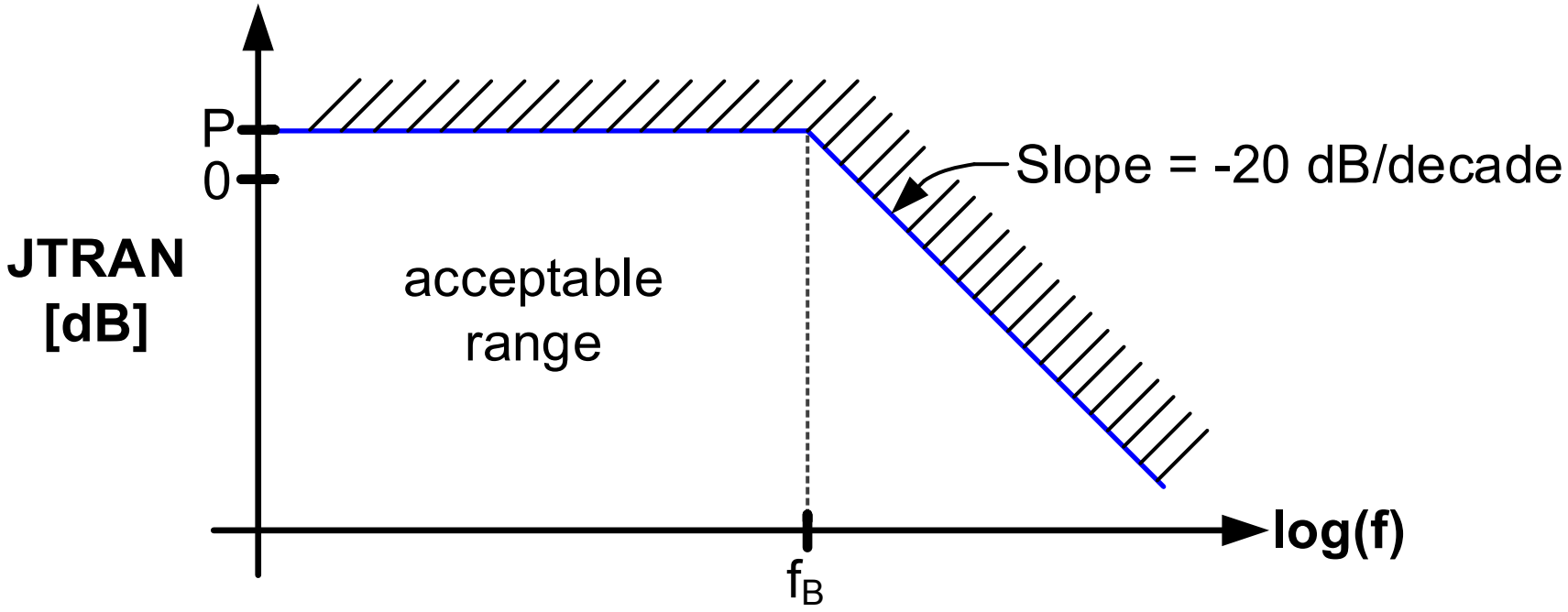
- Increase data input sinusoidal jitter until BER exceeds target

Jitter Transfer (JTRAN)

- Amount of jitter attenuation provided by CDR



JTRAN Mask

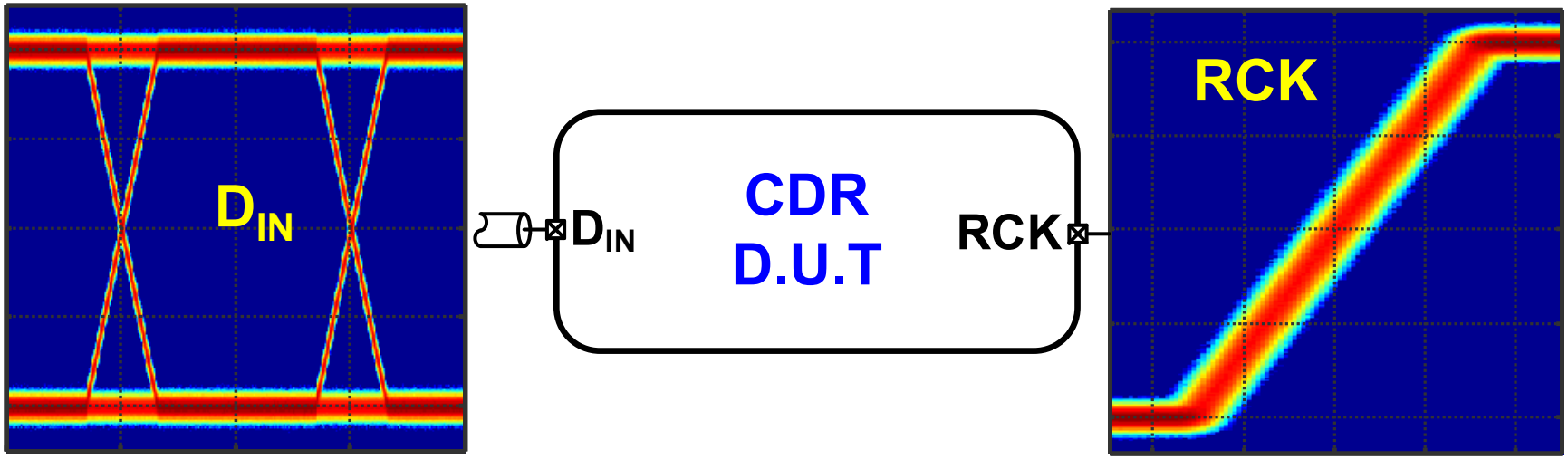


- Modulate data input with sinusoidal jitter and measure resulting output jitter

Jitter Generation (JGEN)

- Amount of output jitter when fed with clean data

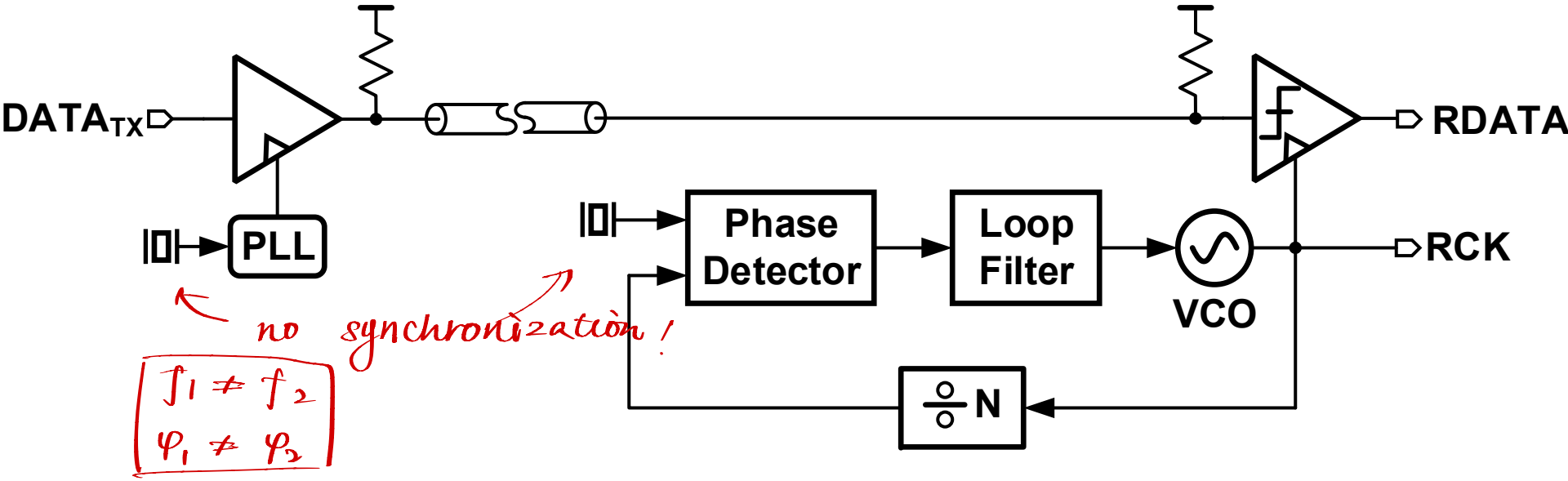
How does jitter getting generated by CDR w/ clean input



Tutorial Roadmap

- Performance metrics
- **Basic architectures**
  - **Linear/Bang-bang**
  - **Digital**
  - **Hybrid**
- Application-specific CDRs
  - Multi-lane chip-to-chip links
  - Repeaters for optical links and active cables
- Summary

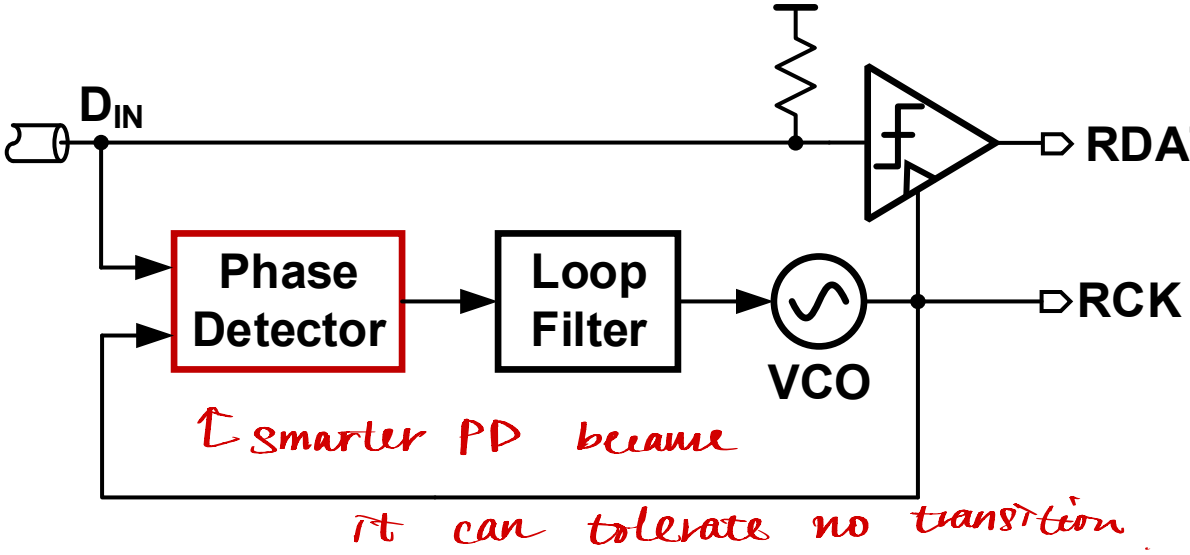
Phase-Locked Loop based CDR

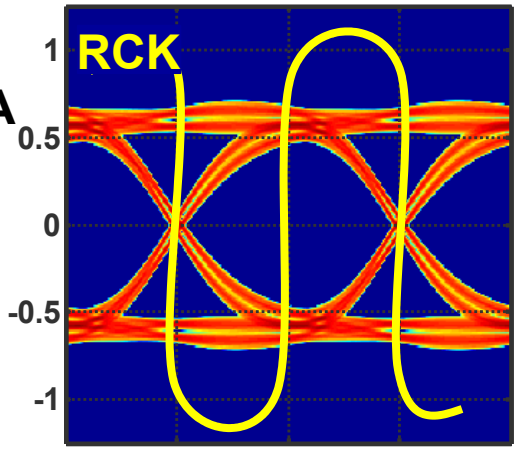


- This **WON'T work** because:
  - Crystal oscillators at TX and RX do not match
  - No phase relationship between received data and RCK

- **Need:** Acquire freq. & phase information from data

PLL-based CDR

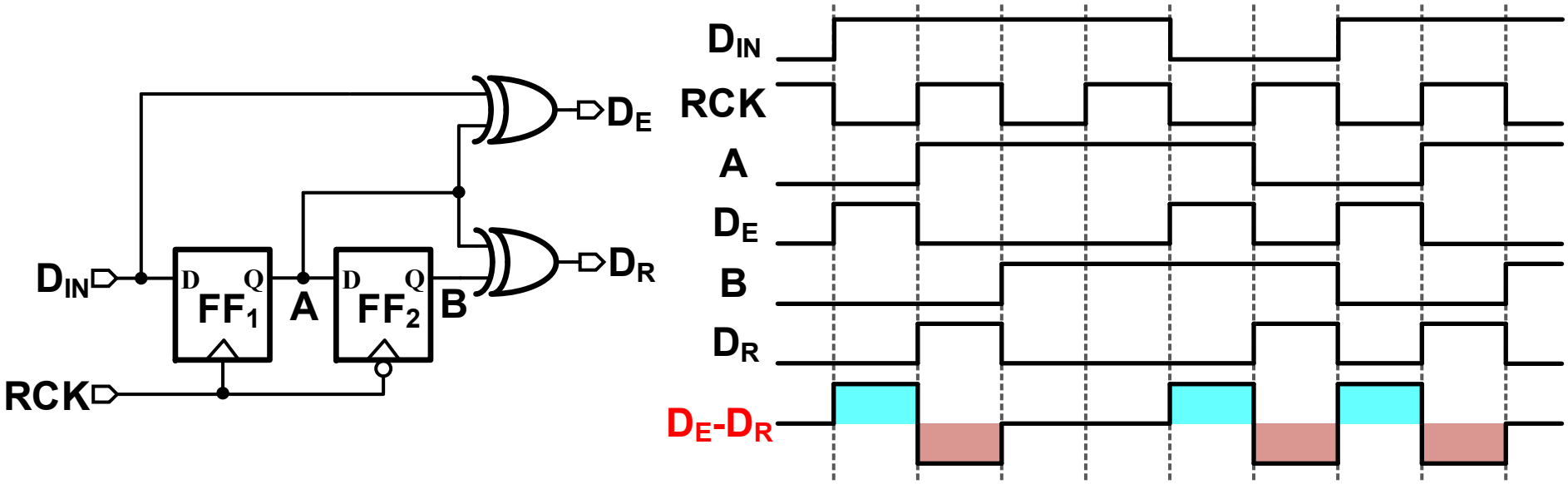




- Phase detector should tolerate missing transitions
- Rest of the building blocks similar to a PLL

- Neg. edge of recovered clock locks to data edge
- Pos. edge samples data in the middle of the eye

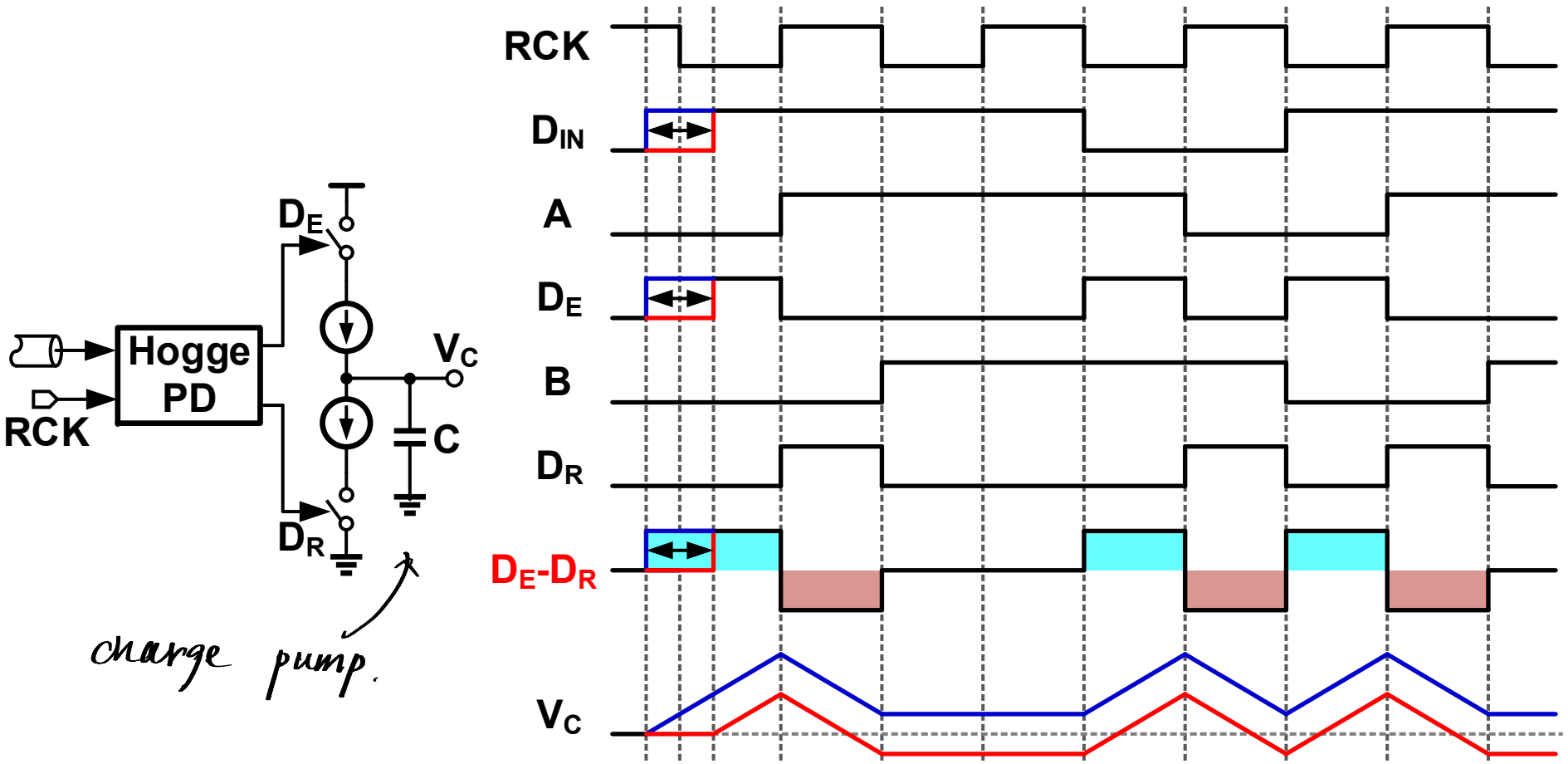
Linear (Hogge) Phase Detector[1]



- Error output (D_E-D_R) is difference of 2 pulses
  - Pulse width of D_E is proportional to phase error
  - Pulse width of D_R is fixed and is equal to $T_{RCK}/2$
- Area under D_E-D_R is proportional to phase error
  - Area is zero when RCK is aligned with D_{IN}

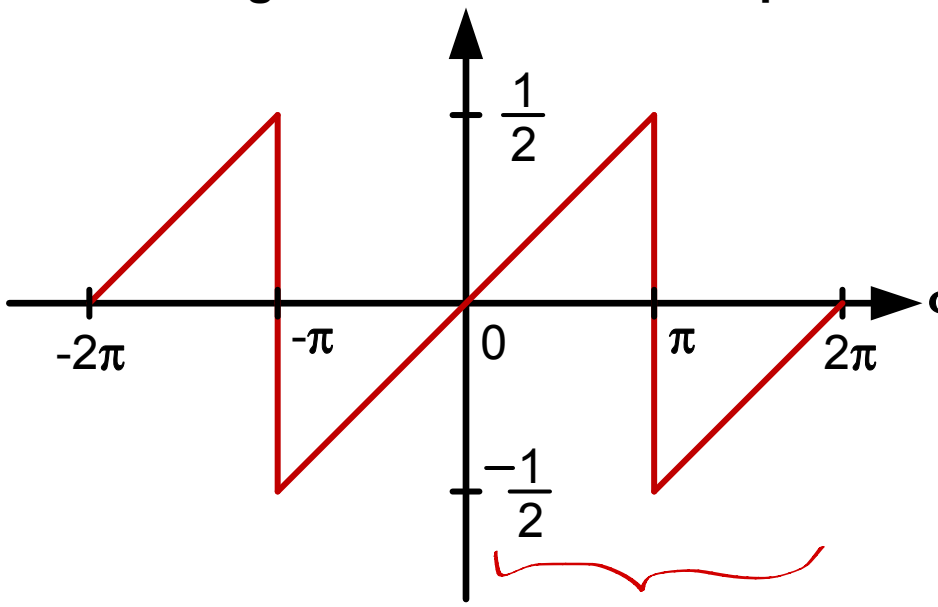
when there is a transition, D_E pulses $\Delta\varphi$, D_R pulses $\frac{T}{2}$.
They are quite if no transition presents. Compare D_E to D_R.

Hogge PD Waveforms



Hogge PD Transfer Function

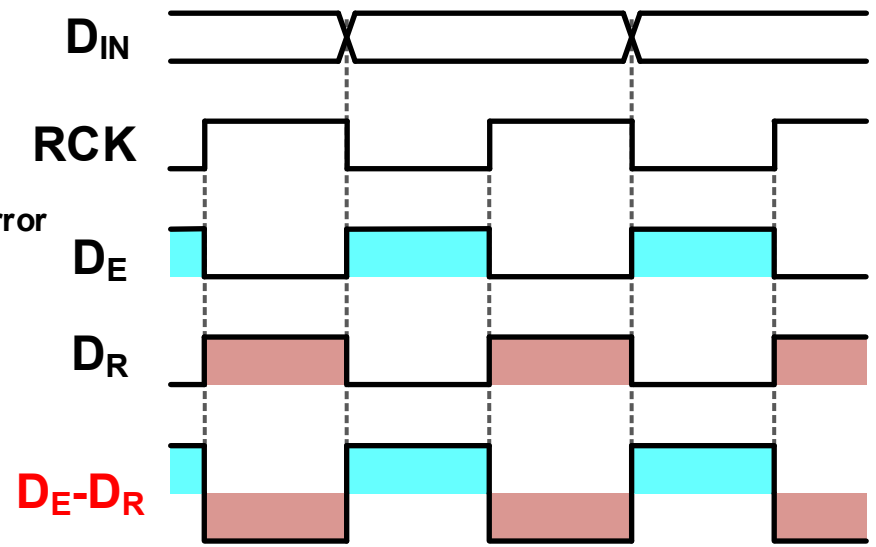
Average Phase Detector Output



$$\text{Linear range} : \pm\pi$$

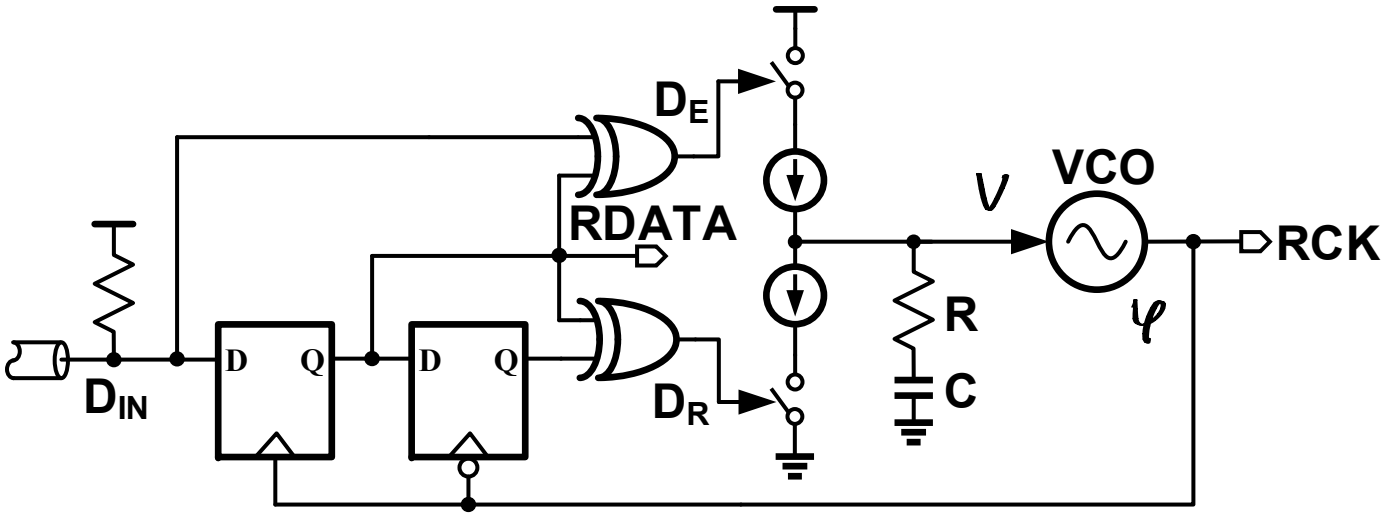
$$\text{Gain } K_{pd} = \frac{1}{2\pi}$$

$\Phi_{Error} = 0$



when Φ_{ERROR} ↗ because ∃ Δf, Hogge PD is not a frequency detector.

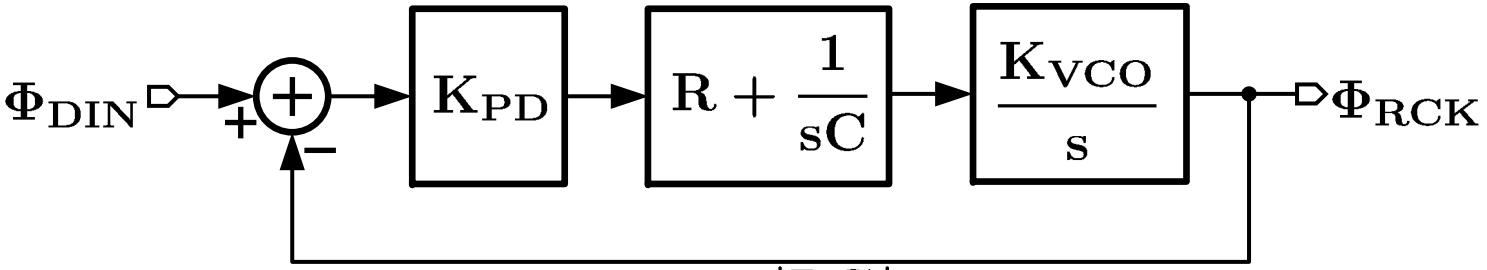
CDR Using Hogge Phase Detector



- Type-II response
  - 2 integrators – one in the loop filter and the other is VCO
- Zero static phase offset (ideally)
  - CP output should be zero in steady state
  - Implies input phase error = 0

most CDR is type 2 because we don't tolerate $\Delta\varphi$ b/w data & clock ← in the middle of the eye.

Choosing Loop Parameters



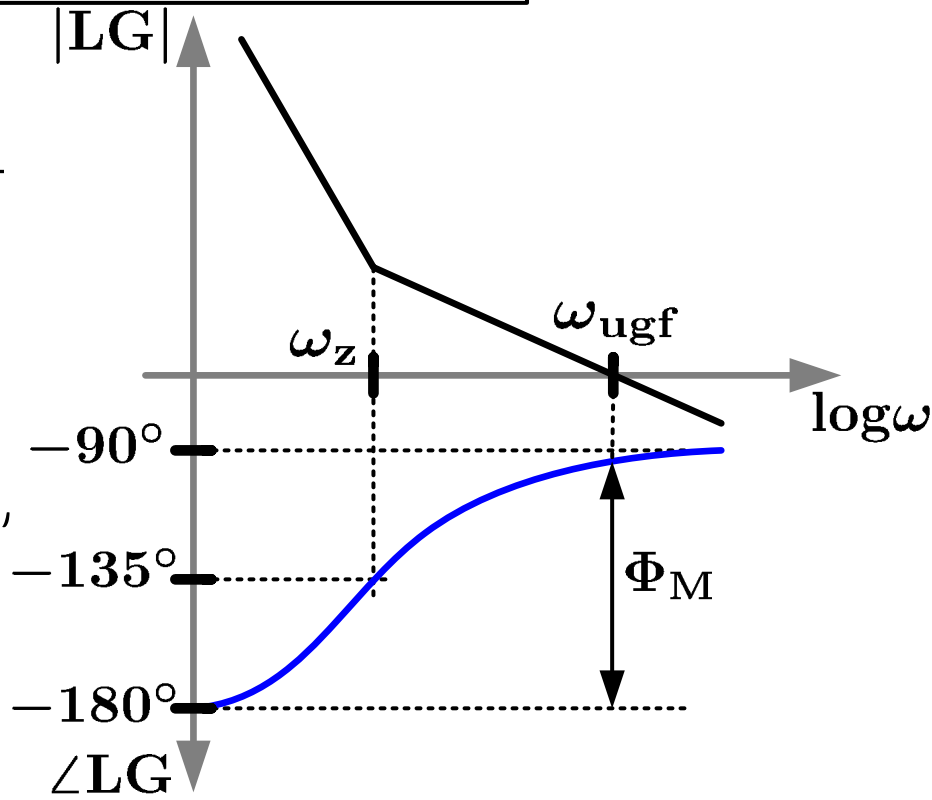
$$LG(s) = K_{PD} \cdot \left(R + \frac{1}{sC}\right) \cdot \frac{K_{VCO}}{s}$$

$$\omega_z = \frac{1}{RC},\ \omega_{p1} = 0,\ \omega_{p2} = 0$$

R ~ few kΩs

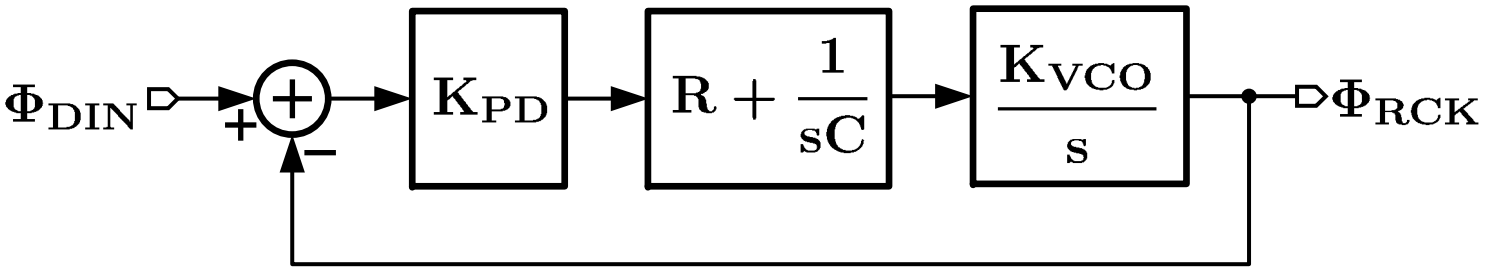
JTRAN BW $\approx \omega_{ugf}$ unit gain freq

$$\Phi_M = \arctan\left(\frac{\omega_{ugf}}{\omega_z}\right)$$



Jitter Transfer Function

Mason's Rule



$$H_{JTRAN}(s) = \frac{\Phi_{RCK}(s)}{\Phi_{DIN}(s)} = \frac{FPG(s)}{1 + LG(s)}$$

$$= \frac{1 + sRC}{1 + sRC + s^2 \cdot \frac{C}{K_{VCO} K_{PD}}}$$

$$\equiv \frac{1 + s/\omega_z}{(1 + s/\omega_{PL})(1 + s/\omega_{PH})}$$

usually $\omega_z \sim \omega_{PL}$

$\omega_z = 1/RC$

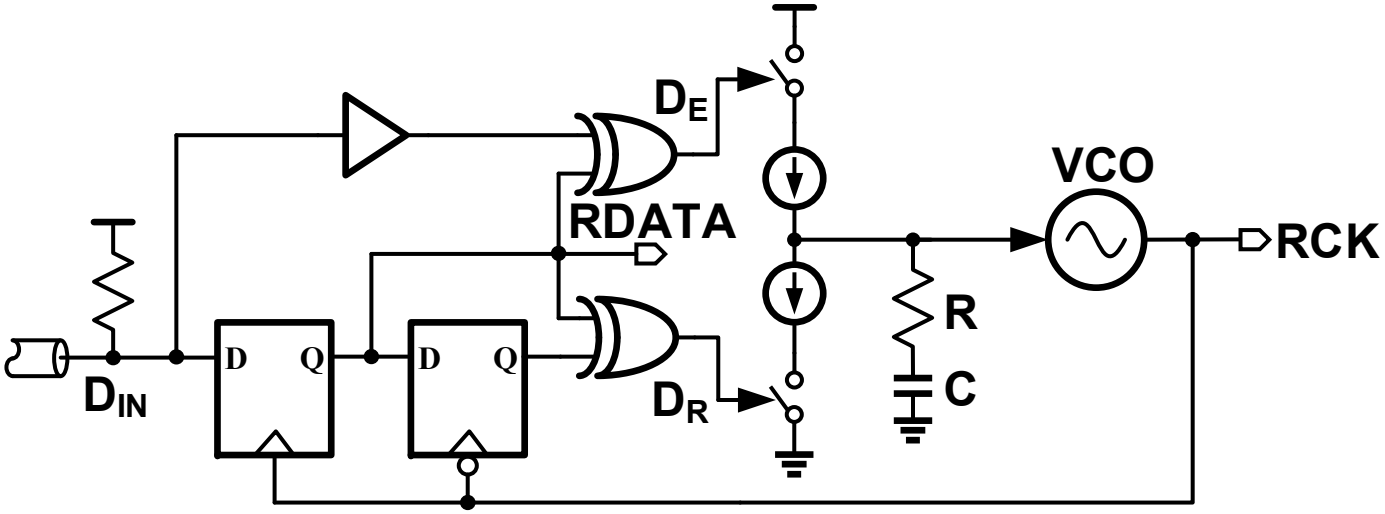
$\omega_{PL} \approx 1/RC$

$\omega_{PH} \approx K_{VCO} \cdot K_{PD} \cdot R$

JTRAN BW $= \omega_{-3dB} \approx \omega_{PH} \approx K_{VCO} \cdot K_{PD} \cdot R$

- usually overdamped.

Linear CDR Drawbacks



- Jitter peaking (large loop filter area)
- Coupled JTRAN and JTOL

  can't choose one over another.
- Hogge PD non-idealities

Jitter Peaking (I)

- Zero in feed-forward path → inevitable peaking

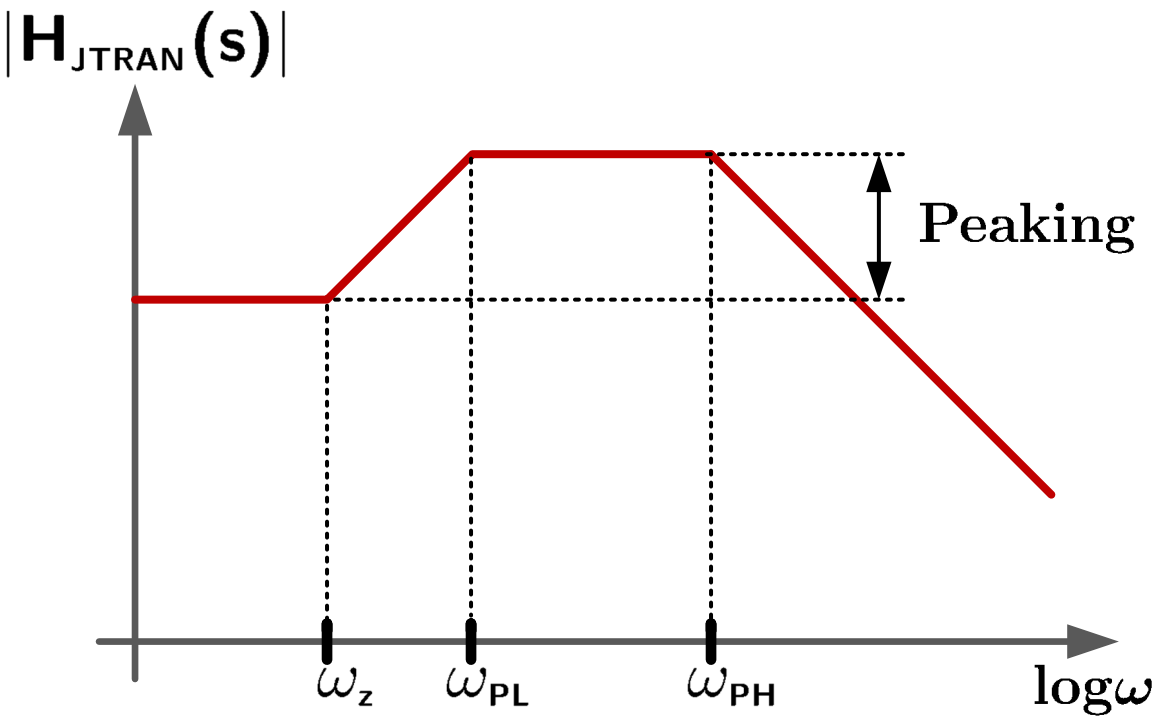
$$H_{JTRAN}(s) = \frac{1 + sRC}{1 + sRC + s^2 \cdot \frac{C}{K_{VCO} K_{PD}}}$$

ω_z has to be less than ω_{PL}.

$$\omega_z = 1/RC$$

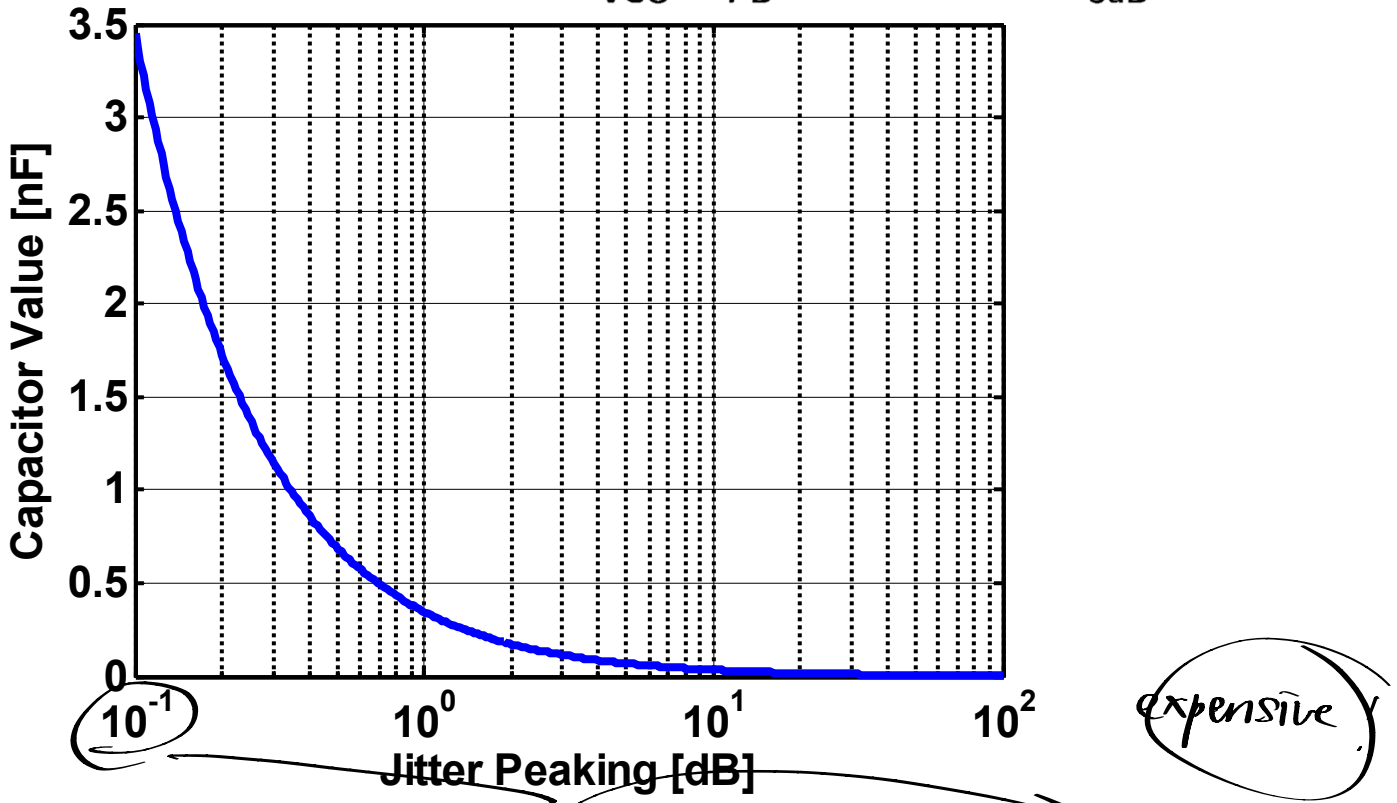
$$\omega_{PL} \approx 1/RC$$

$$\omega_{PH} \approx K_{VCO} \cdot K_{PD} \cdot R$$



Jitter Peaking (II)[2]

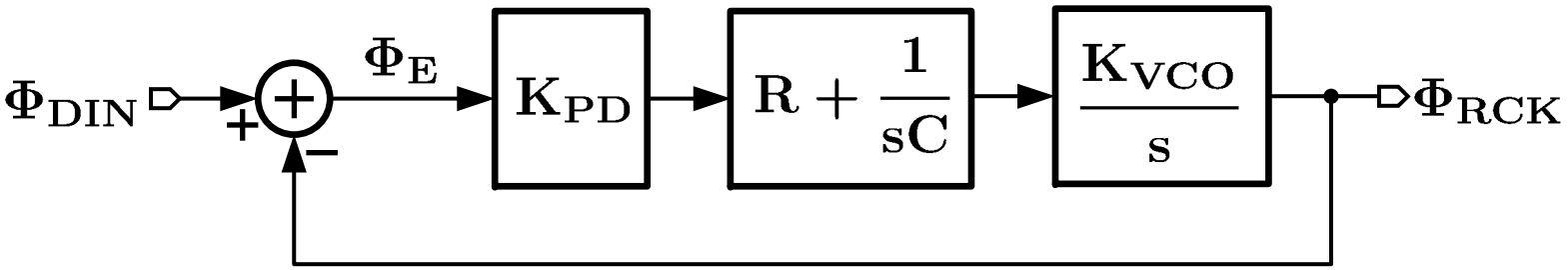
$$\text{Jitter Peaking [dB]} \approx \frac{8.686}{K_{VCO}K_{PD}CR^2} \approx \frac{8.686}{\omega_{-3dB}CR}$$



- BW = 4MHz, R = 1kΩ & 0.1dB peaking, C ~ 3.5nF

repeaters : can't tolerate any jitter peaking.

Jitter Tracking



$$H_{JTRACK}(s) = \frac{\Phi_E(s)}{\Phi_{DIN}(s)} = \frac{1}{1 + LG(s)}$$

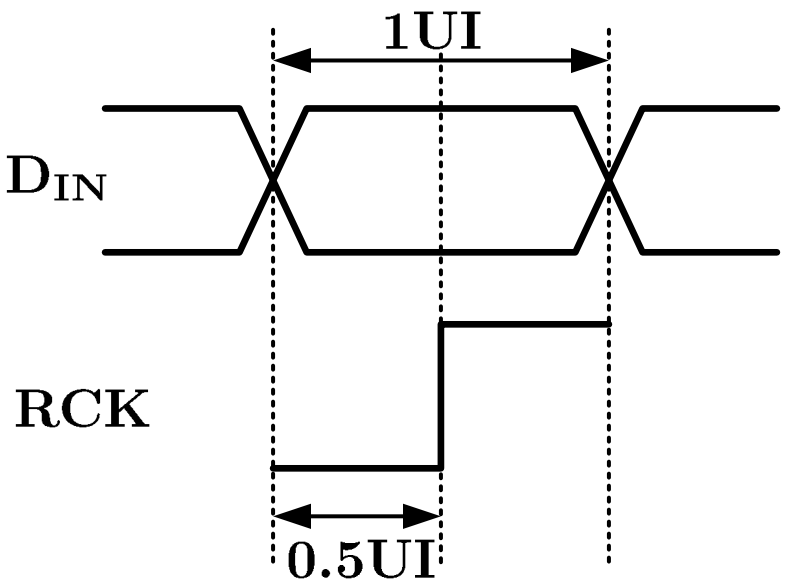
$$= \frac{s^2 \cdot \frac{C}{K_{VCO}K_{PD}}}{1 + sRC + s^2 \cdot \frac{C}{K_{VCO}K_{PD}}}$$

$$\equiv \frac{s^2/\omega_{PL}\omega_{PH}}{(1 + s/\omega_{PL})(1 + s/\omega_{PH})}$$

$$\text{JTRACK BW} = \omega_{-3dB} \approx \omega_{PH} \approx K_{VCO} \cdot K_{PD} \cdot R$$

When jitter $f \ll$ BW, fully tracked.

Jitter Tolerance (JTOL) (I)



$$|\Phi_E| < 0.5\,UI$$

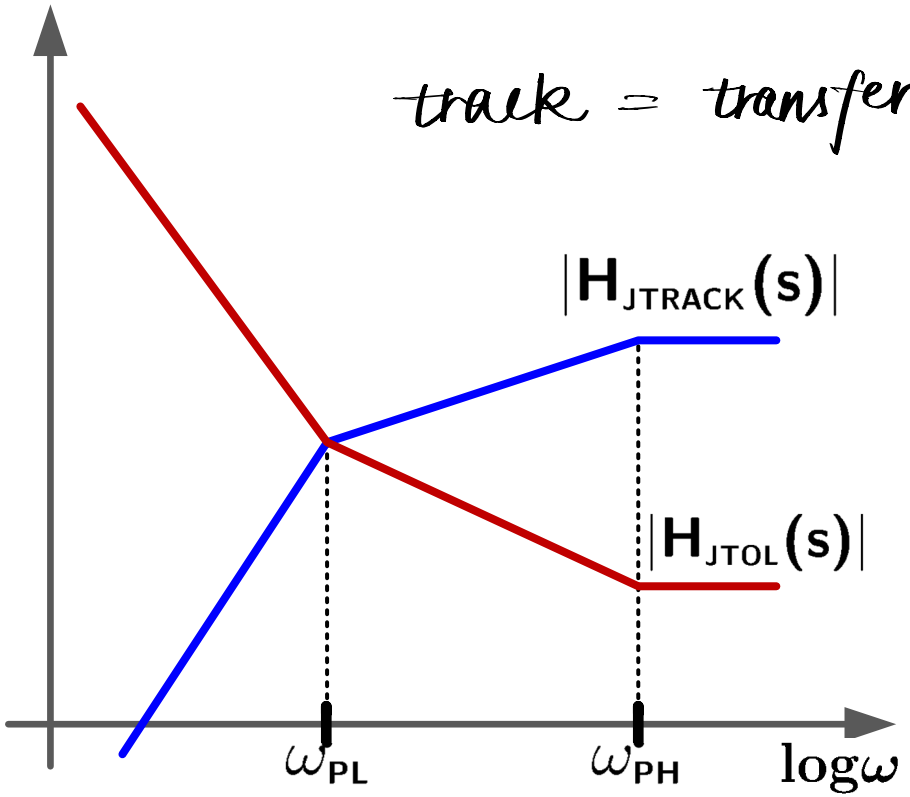
$$\Phi_{DIN} \times H_{JTRACK}(s) < 0.5\,UI$$

$$\Longrightarrow \quad \Phi_{DIN} < \frac{0.5\,UI}{H_{JTRACK}(s)}$$

$$H_{JTOL}(s) = \frac{0.5}{H_{JTRACK}(s)}$$

$$H_{JTOL}(s) = \frac{0.5\,(1 + s/\omega_{PL})\,(1 + s/\omega_{PH})}{s^2/\omega_{PL}\omega_{PH}}$$

Jitter Tolerance (JTOL) (II)

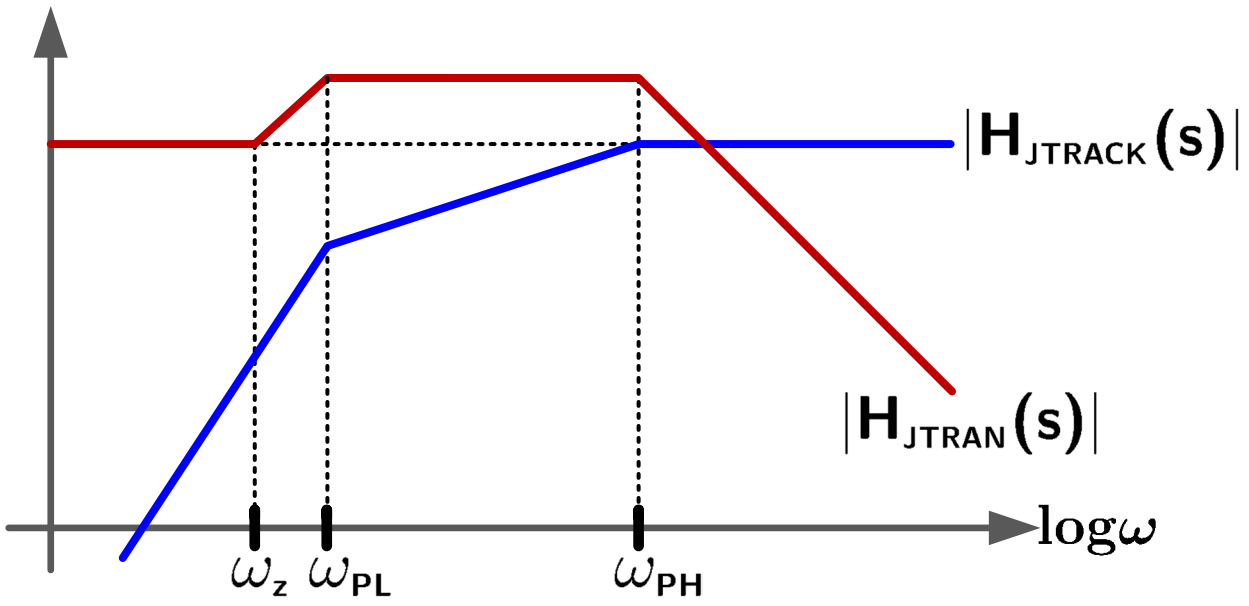


- JTOL improves w/ better jitter tracking
  - Better jitter tracking → wider JTRAN bandwidth!

Coupled JTRAN/JTOL Behavior

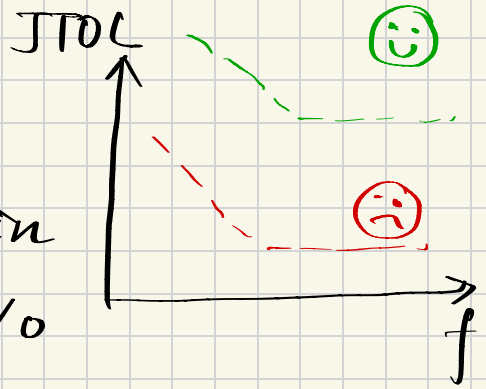
$$H_{JTRAN}(s) = \frac{1 + sRC}{1 + sRC + s^2 \cdot \frac{C}{K_{VCO} K_{PD}}}$$

$$H_{JTRACK}(s) = \frac{s^2 \cdot \frac{C}{K_{VCO} K_{PD}}}{1 + sRC + s^2 \cdot \frac{C}{K_{VCO} K_{PD}}}$$



- Both JTRAN and JTOL are governed by ω_{PH}

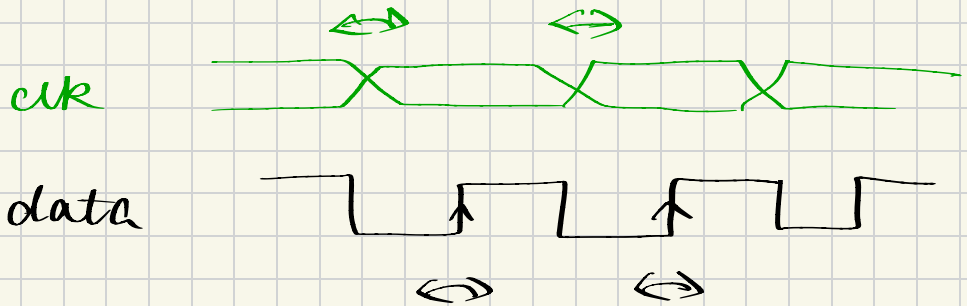
* JTOL



· usually JTOL is the larger the better since it characterize how much jitter in the data stream can CDR tolerate w/o causing a bit error.

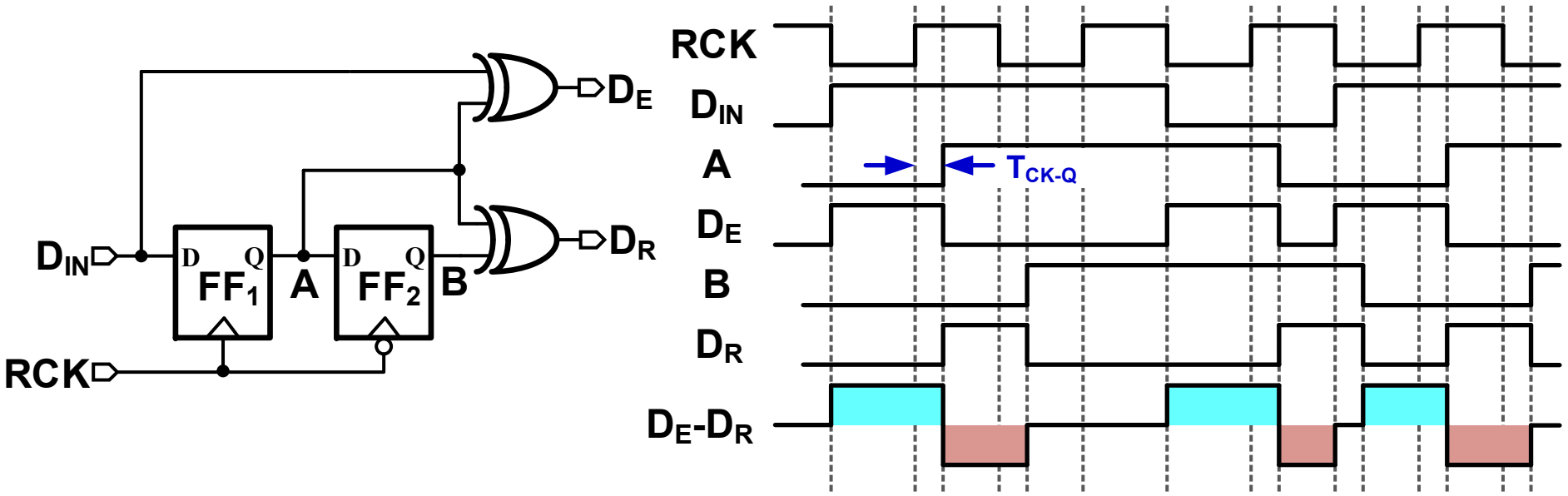
* Jtran

· however, this does require the recovered clock to "track" the jittery data in order to track the behavior well.



△ this can cause the recovered clock to be jittery, or even sometimes missing edges.

Hogge PD Non-idealities: Offset[2]

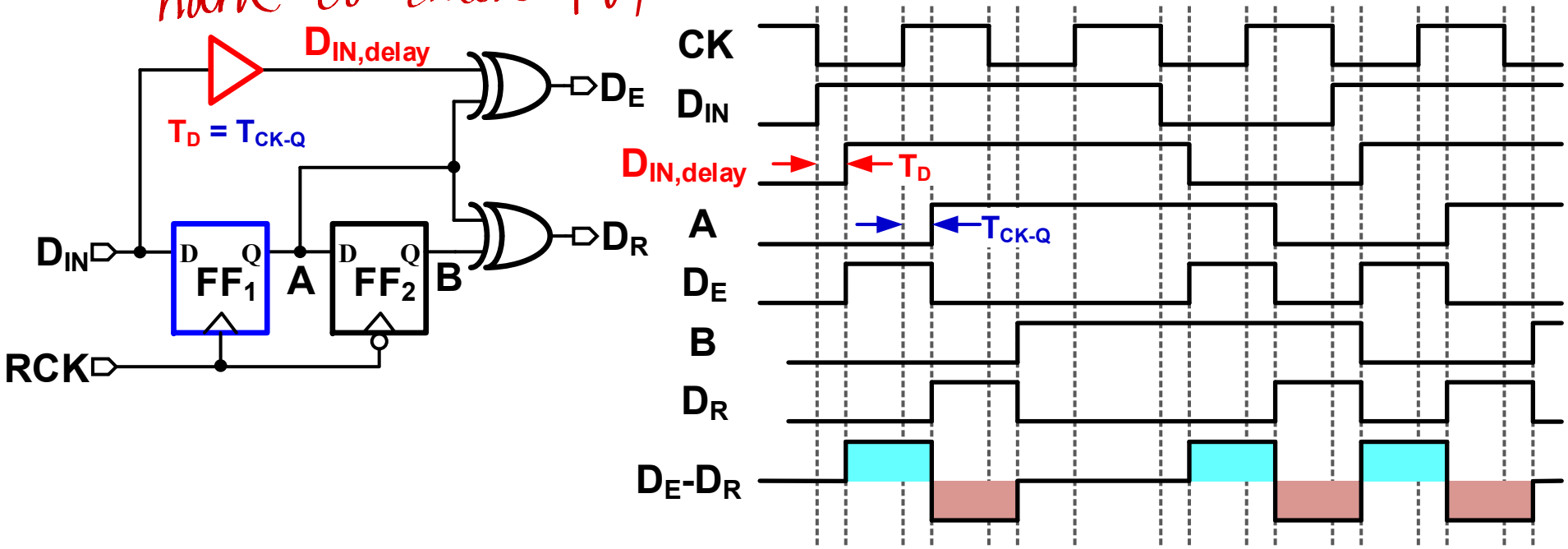


- FF1 clock-to-Q delay introduces phase offset

causing locking errors.

Hogge PD Offset Mitigation[2]

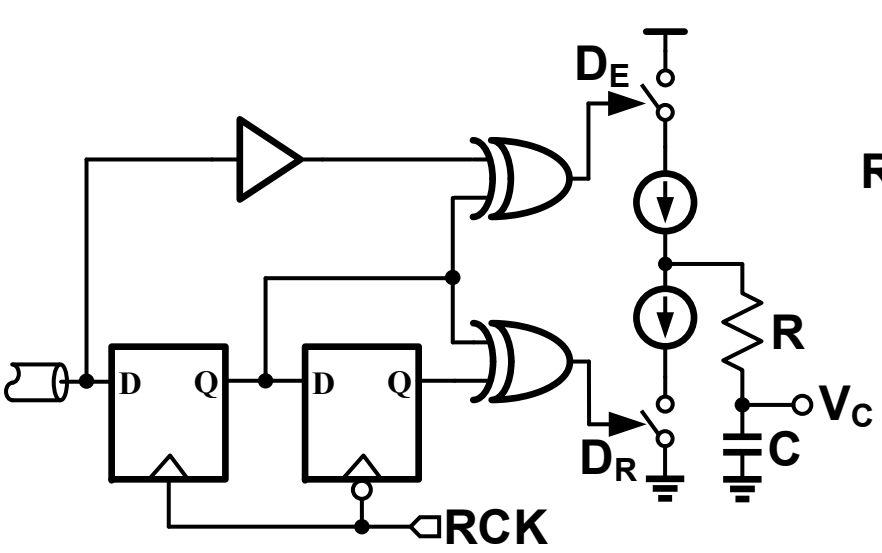
hard to track PVT

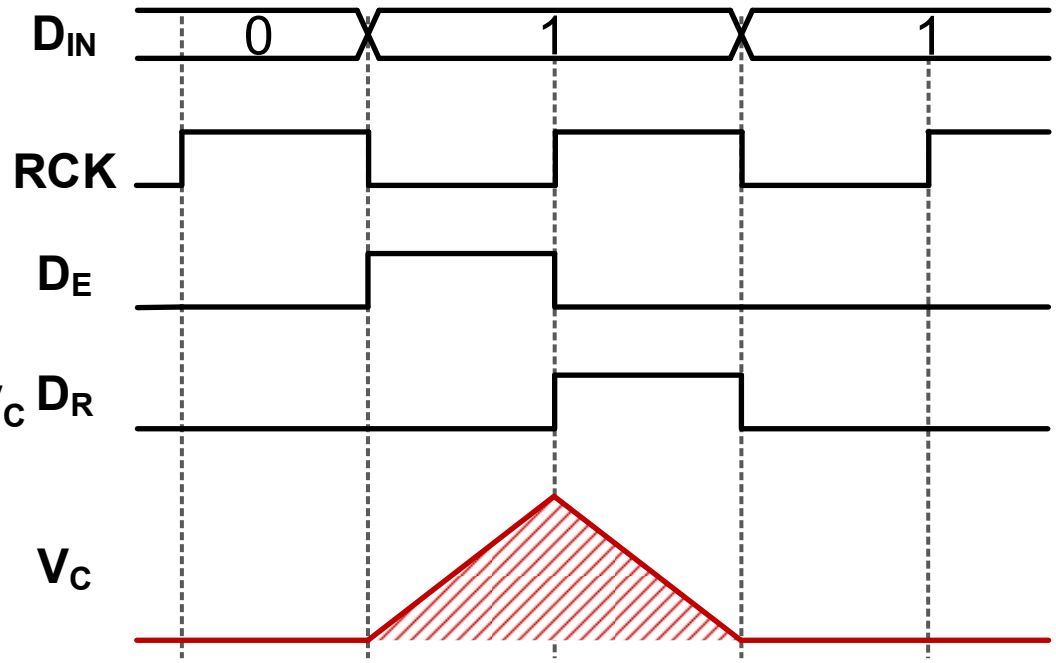


- FF1 clock-to-Q delay introduces phase offset
- FF1 delay compensated by inserting buffer
  - T_D may not track T_{CK-Q} across supply and temperature
  - Generating small well controlled T_D is also difficult

• main reason Hogge PD not used in high f.

Hogge PD Non-idealities: DDJ[2]





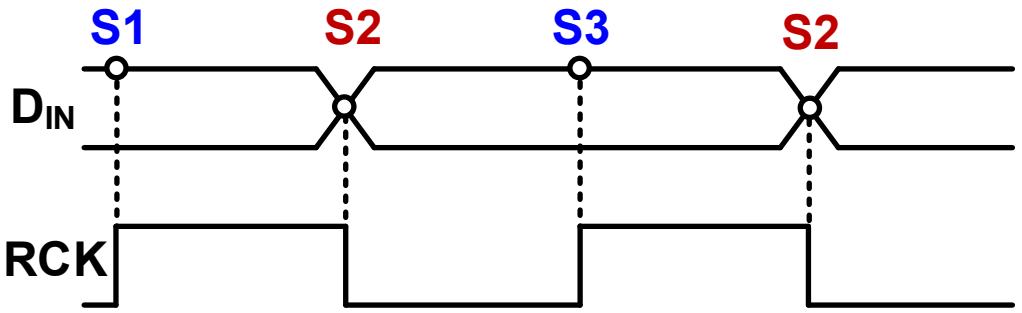
causing VCO f↗

- D_E/D_R pulses not aligned in time
  - "Tri-wave" on V_C causes Data Dependent Jitter (DDJ)
- See [2] for modified Hogge PD to mitigate DDJ

Bang-Bang Phase Detector (I)

- Can we detect phase error from sampled data?

Phase error = 0

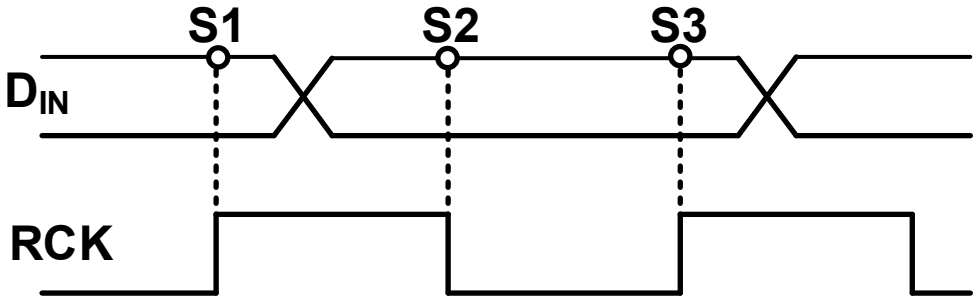


S1 and S3 are data samples

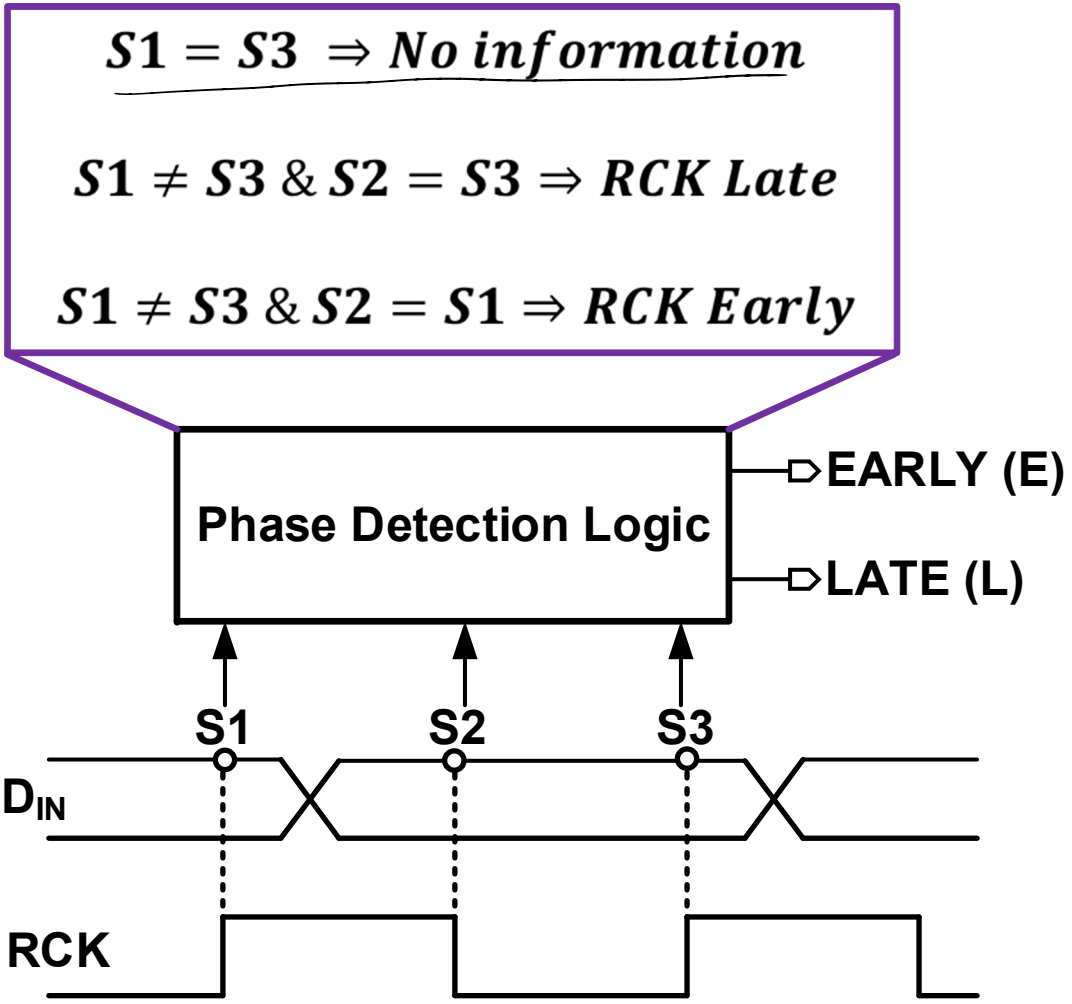
S2 is edge sample

late : S2 = S3

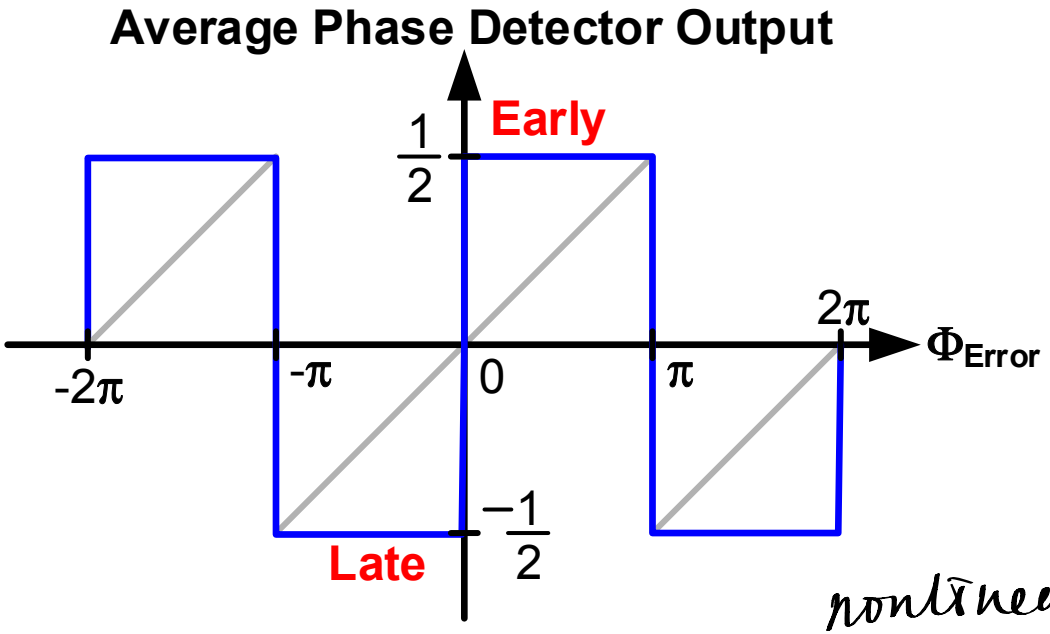
Phase error ≠ 0



Bang-Bang Phase Detector (II)[3]



BBPD Characteristics: w/o Jitter

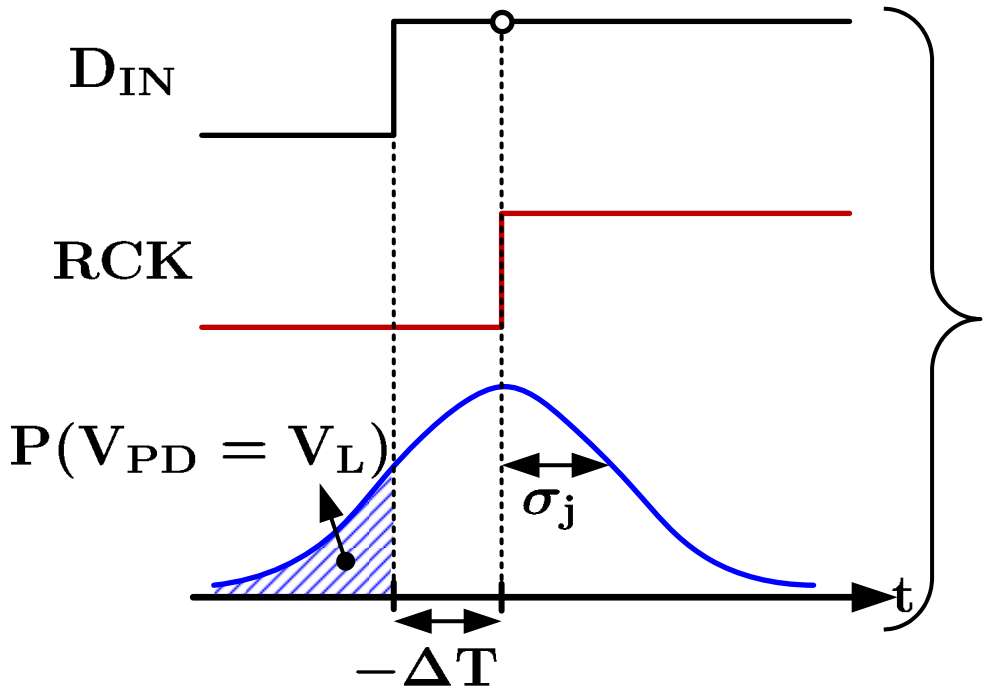


nonlinear

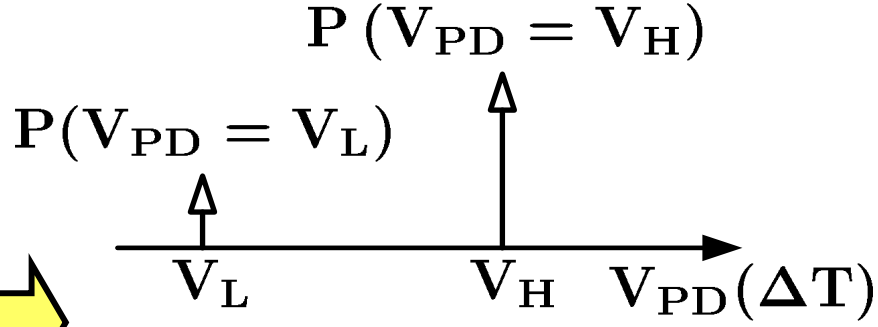
Useful range : $\pm\pi$

Gain $K_{PD}|_{\Delta T=0} = \infty$

BBPD Characteristics: w/Jitter (I)[4]



Discrete PDF of BBPD output



$$P(V_{PD} = V_L) = \int_{-\infty}^{-\Delta T} p(x)dx$$

$$P(V_{PD} = V_H) = \int_{-\Delta T}^{\infty} p(x)dx$$

$$\overline{V_{PD}(\Delta T)} = V_L \cdot P(V_{PD} = V_L) + V_H \cdot P(V_{PD} = V_H)$$

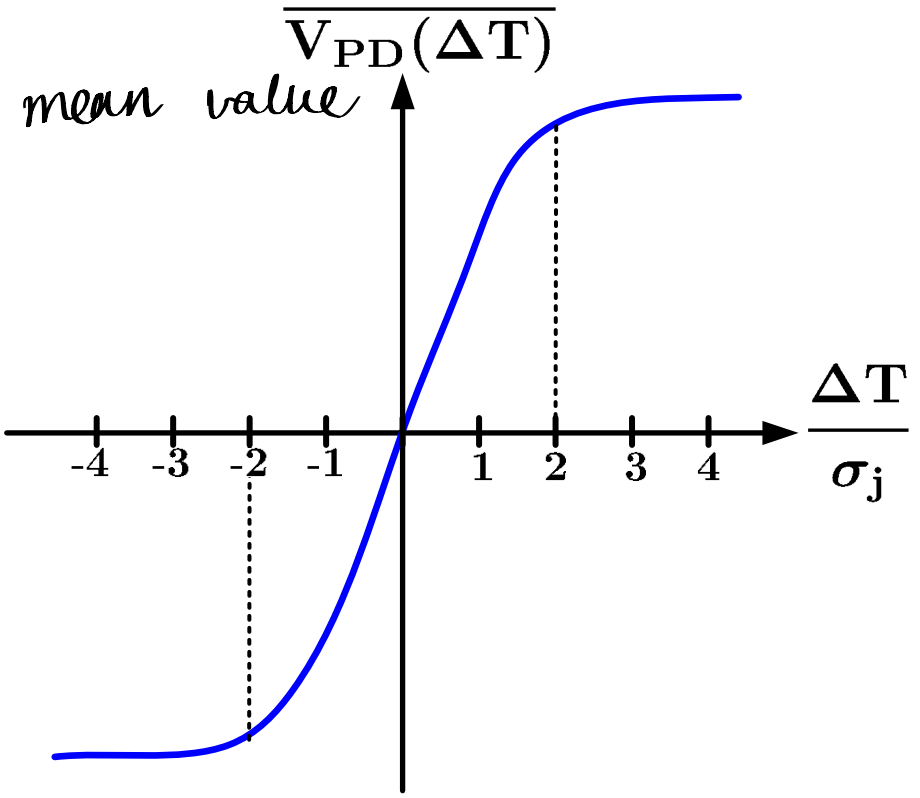
BBPD Characteristics: w/ Jitter (II)

$$\overline{V_{PD}(\Delta T)} = 2V_o \cdot erf\left(\frac{\Delta T}{\sigma_j}\right)$$

$$erf(x) = \frac{1}{\sqrt{2\pi}} \int_0^x e^{-y^2} dy$$

$$\text{Gain } K_{PD}|_{\Delta T=0} = \frac{2V_o}{\sqrt{2\pi}\sigma_j}$$

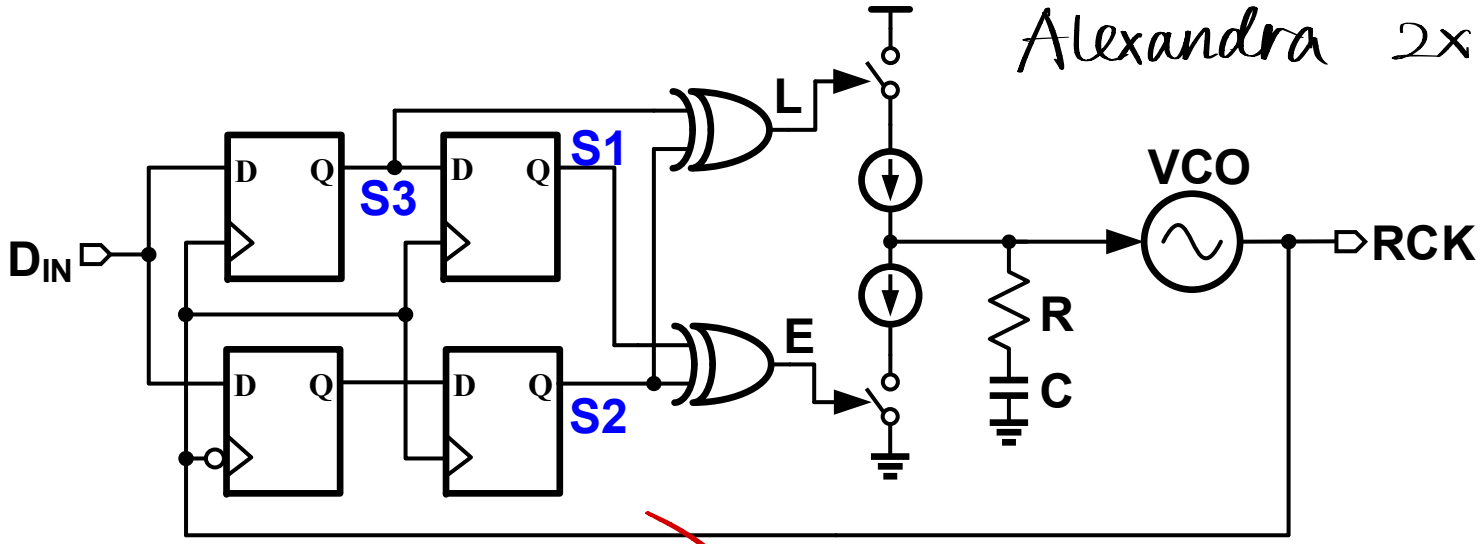
$$\text{Linear range} : \pm 2\sigma_j$$



Linearized due to jitter.

$$K_{PD} = \frac{d\overline{V_{PD}(\Delta T)}}{d\Delta T} = \frac{2V_o}{\sqrt{2\pi}\sigma_j} e^{\left(-\frac{\Delta T}{\sqrt{2}\sigma_j}\right)^2}$$

Full-rate Bang-Bang CDR



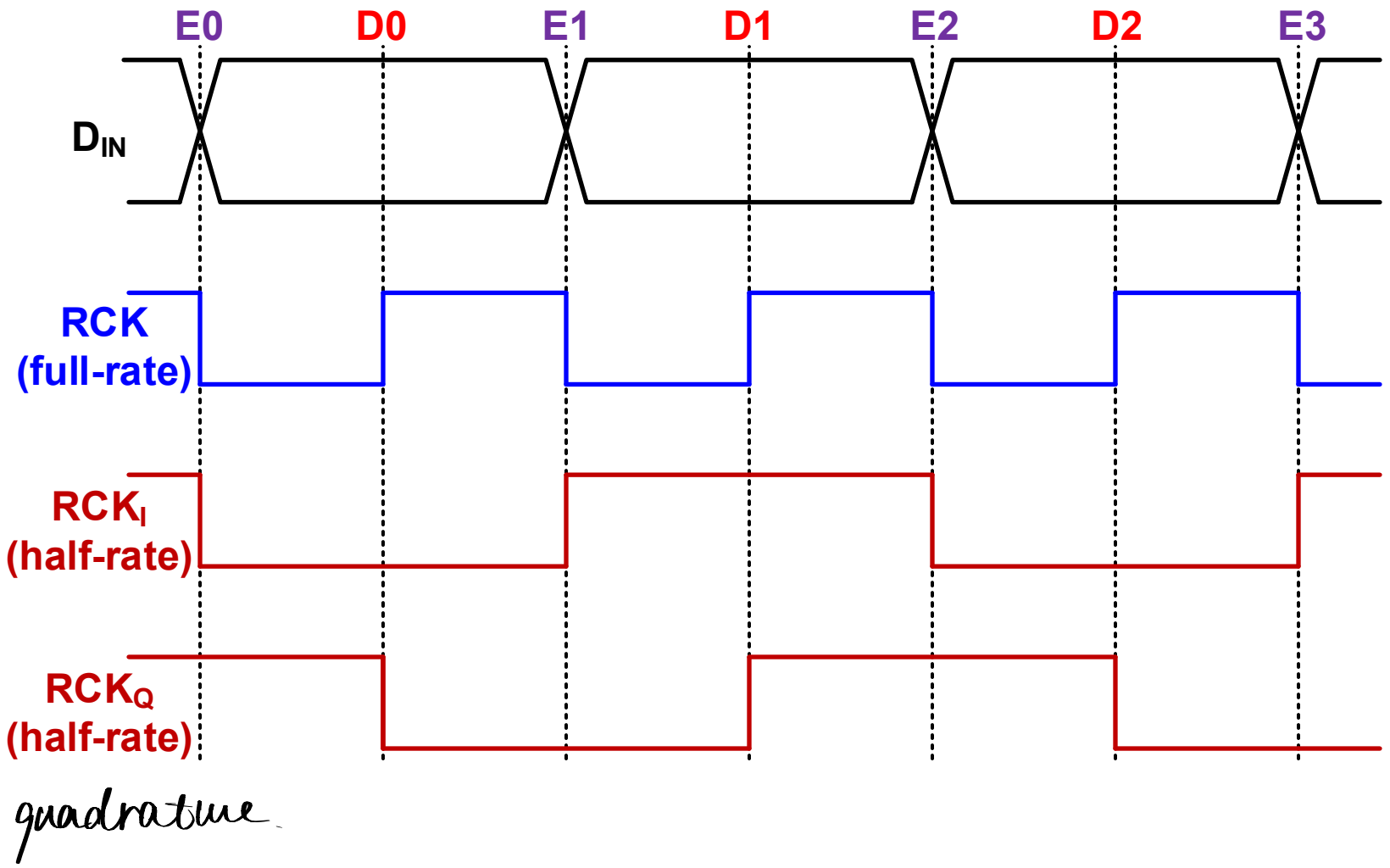
- Type-II response
- Near-zero static phase offset
- Insensitive to charge-pump non-idealities
- VCO & PD operate at full-rate ($F_{VCO} = F_{DIN}$)
  - Could become a speed bottleneck
  - Solution: Half-rate bang-bang CDR

because Kpp is large!

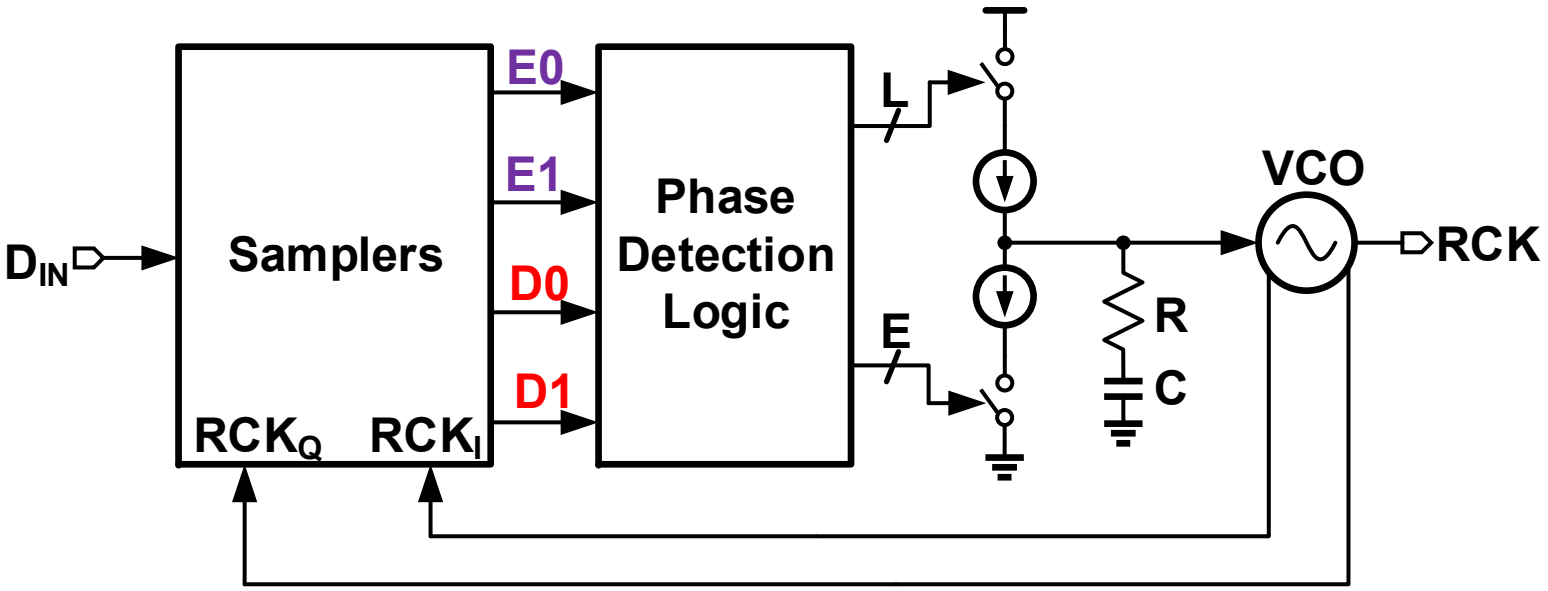
might be a PDK limitation

sub-rate CDR

Half-rate CDR Waveforms

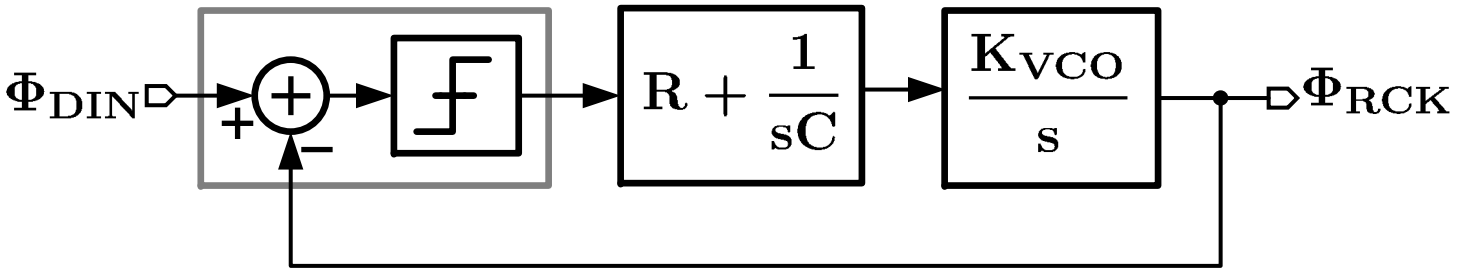


Half-Rate Bang-Bang CDR



- Topology same as full-rate architecture
  - Same phase detection logic as full-rate
- Requires quadrature VCO
- Lower loop update rate → higher loop latency

Choosing Loop Parameters[5]



$$\text{Damping factor } \xi = \frac{\Delta\Phi_{RCK} \text{ due to prop. path}}{\Delta\Phi_{RCK} \text{ due to integ. path}} = \frac{2RC}{T_{UPDATE}} \gg 1$$

- BBPD makes the loop non-linear
  - Cannot use transfer function analysis
  - Loop gain is infinite → unstable in "linear sense"
- Ensure stability by choosing large damping factor
  - Relatively independent proportional and integral paths

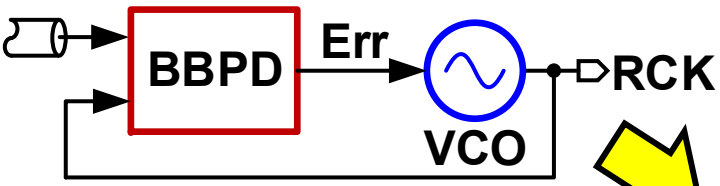
Bang-Bang CDR Drawbacks

- Coupled JTRAN and JTOL
- Jitter peaking
- Large loop filter area

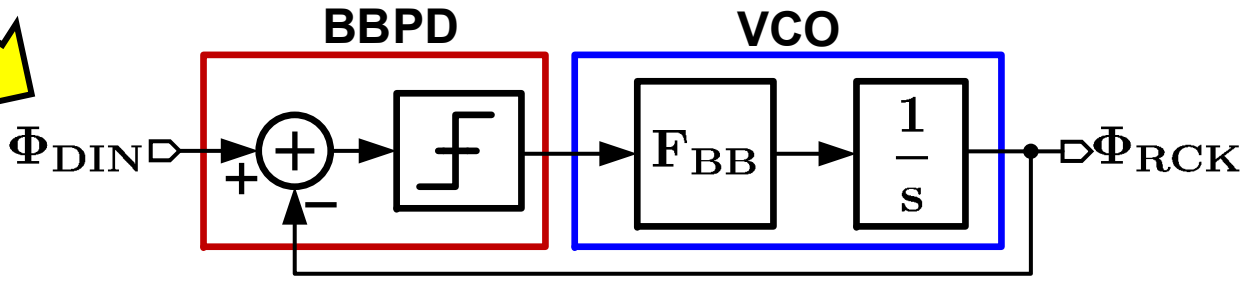
} Similar to linear CDR

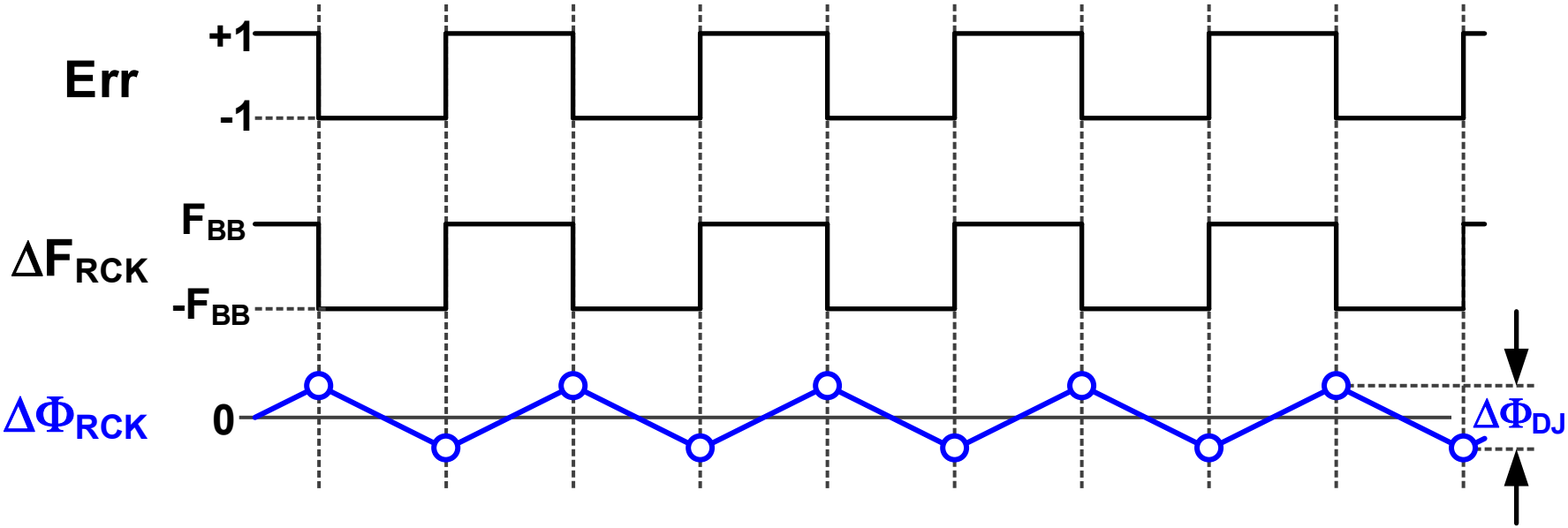
- **JGEN caused by limit cycles** (nonlinear behavior)
- **JTRAN dependence on input jitter**

Steady-State Limit Cycles (I)

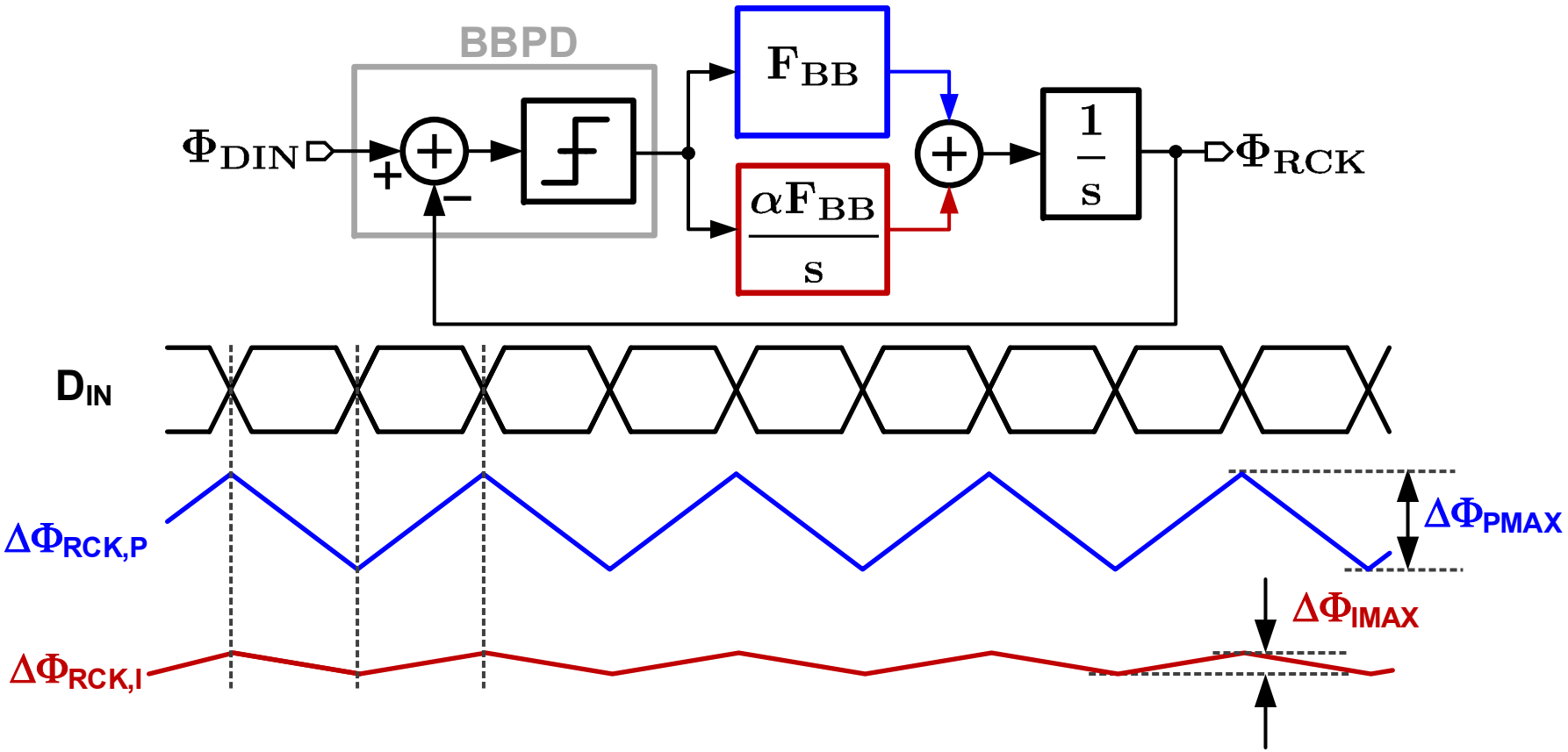


bounded limit cycle.





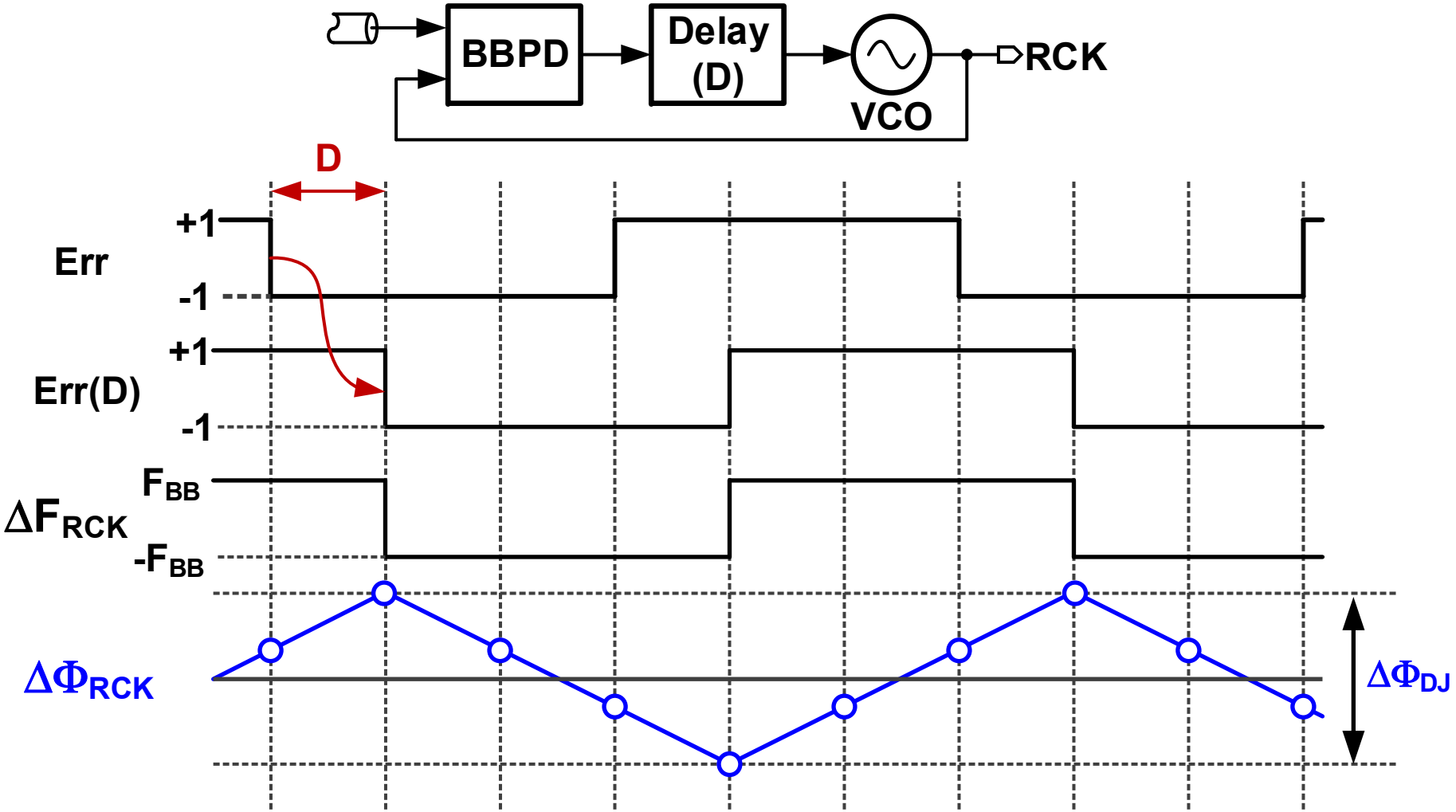
Steady-State Limit Cycles (II)



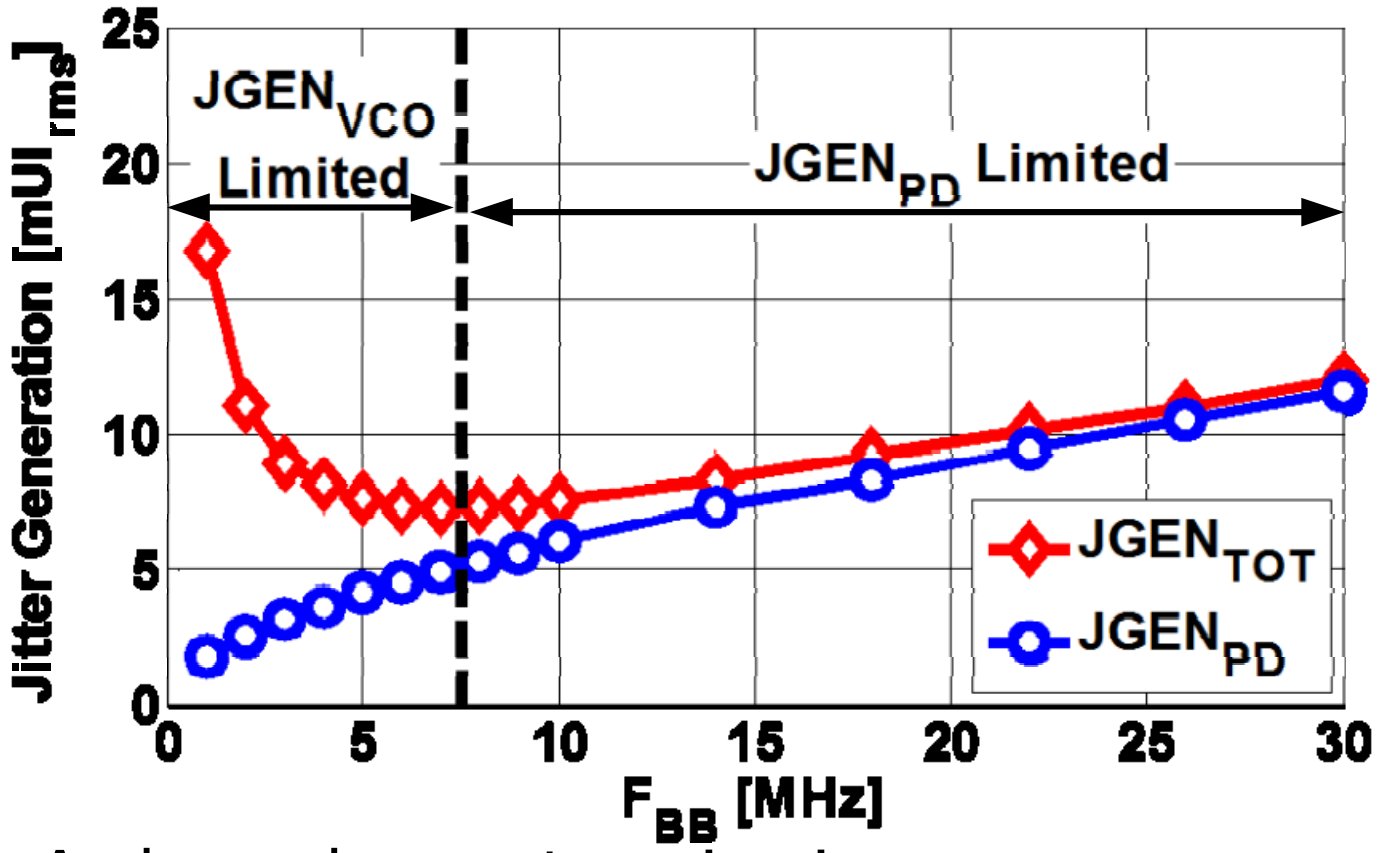
Proportional path dominates dithering jitter

I path suppress low f drifts

Loop Delay Increases JGEN



JGEN vs. Bang-Bang Step Size



- As bang-bang step size increases:
  - Contribution of PD noise to output noise increases
  - Contribution of VCO noise to output noise decreases

JTRAN Dependence on Jitter

$$\text{JTRAN BW} \approx K_{PD} \cdot K_{P} \cdot K_{VCO}$$

$$\text{Gain } K_{PD}|_{\Delta T=0} = \frac{2V_o}{\sqrt{2\pi}\sigma_j} \implies \text{JTRAN BW} \propto \frac{1}{\sigma_j}$$

- JTRAN is inversely proportional to input jitter
  - Difficult to predict *a priori*
- Set JTRAN for minimum input jitter condition
  - Makes it more susceptible to VCO phase noise

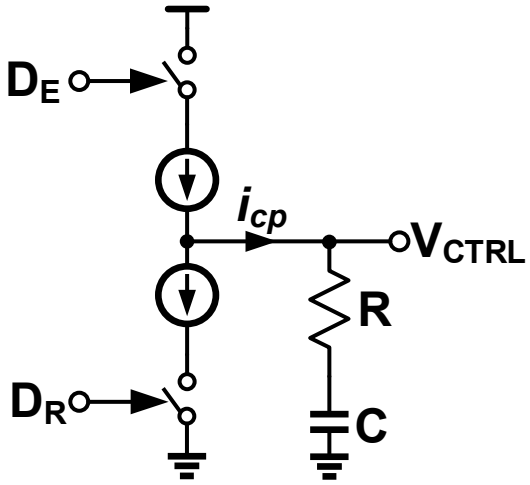
Tutorial Roadmap

- Performance metrics
- **Basic architectures**
  - **Linear/Bang-bang**
  - **Digital**
  - **Hybrid**
- Application-specific CDRs
  - Multi-lane chip-to-chip links
  - Repeaters for optical and active cables
- Summary

Eliminating Loop Filter Capacitor

Just like digital PLL

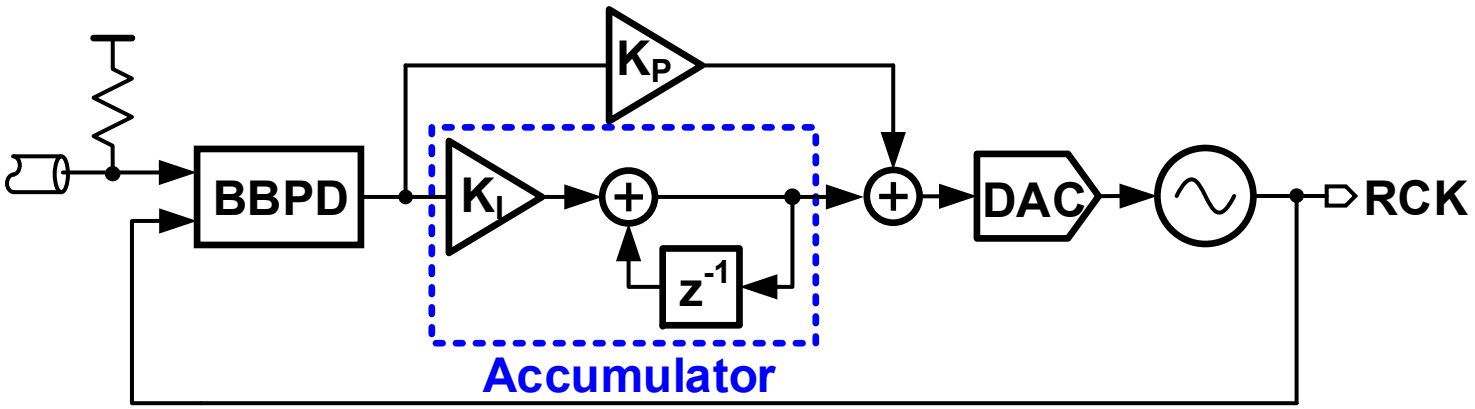
- Map CP + LF into digital domain directly



$$i_{cp}\mathrm{R} + \frac{i_{cp}}{\mathrm{C}s} \Rightarrow i_{cp}\mathrm{R} + \frac{i_{cp}\mathrm{T}}{\mathrm{C}}\frac{z^{-1}}{1-z^{-1}}$$

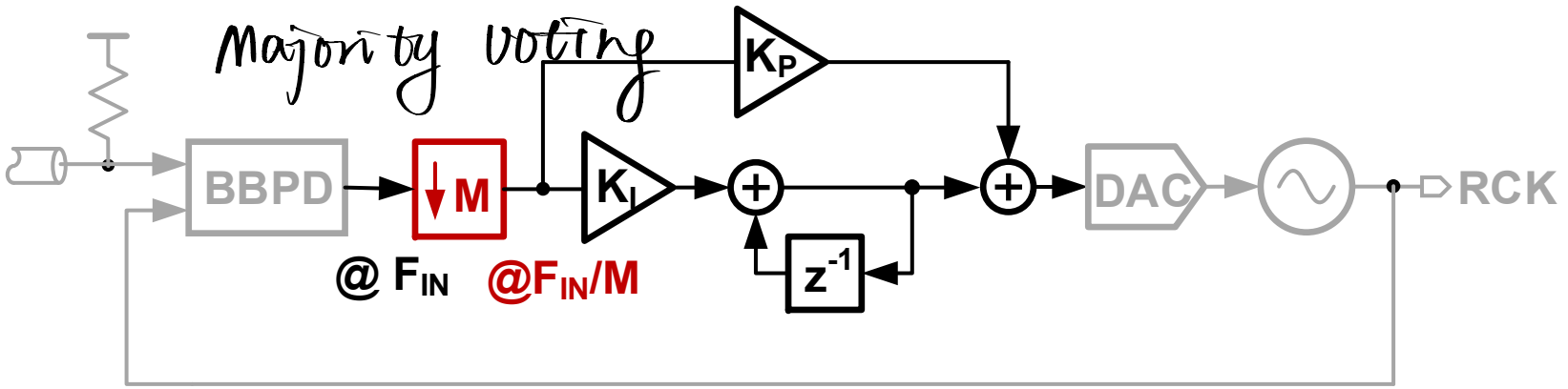
- Digital accumulator replaces loop filter capacitor
  - Large time constant with small area
  - Infinite DC gain → ideal Type-II behavior
  - PVT insensitive
  - Easy to reconfigure for loop dynamics control

Simple Digital CDR[6]



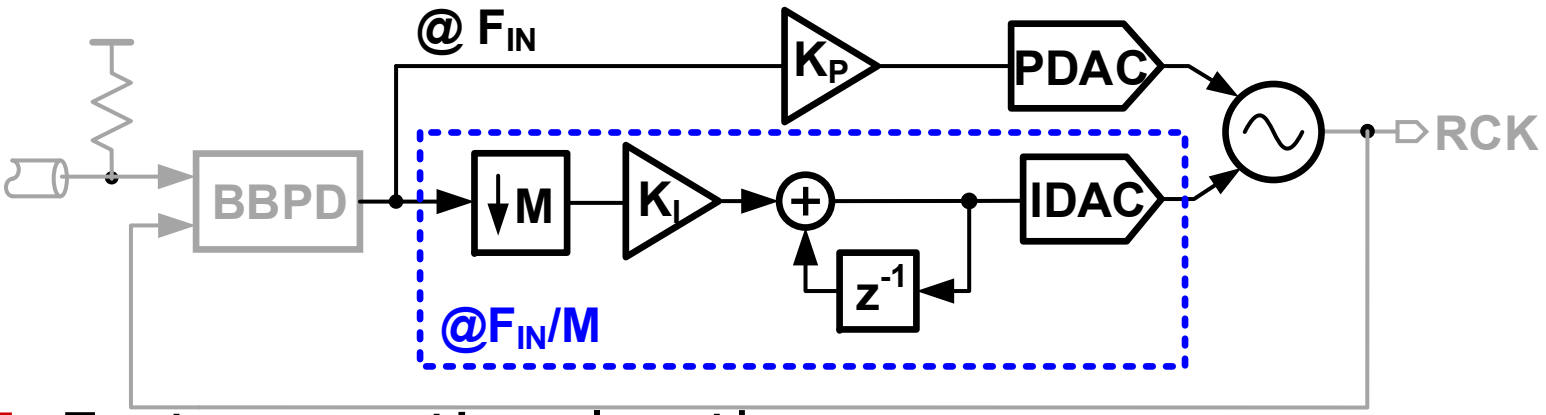
- Loop filter must operate at data rate
- **Need:**
  - Wide operand high-speed adders
  - High speed/resolution **D**igital to **A**nalog **C**onverter (**DAC**)

Reducing Speed Requirements (I)



- Decimation eases speed requirements
- Lower update rate → increases loop latency
  - Loop latency increases dithering jitter
- **Observation:** Proportional path dominates jitter

Reducing Speed Requirements (II)

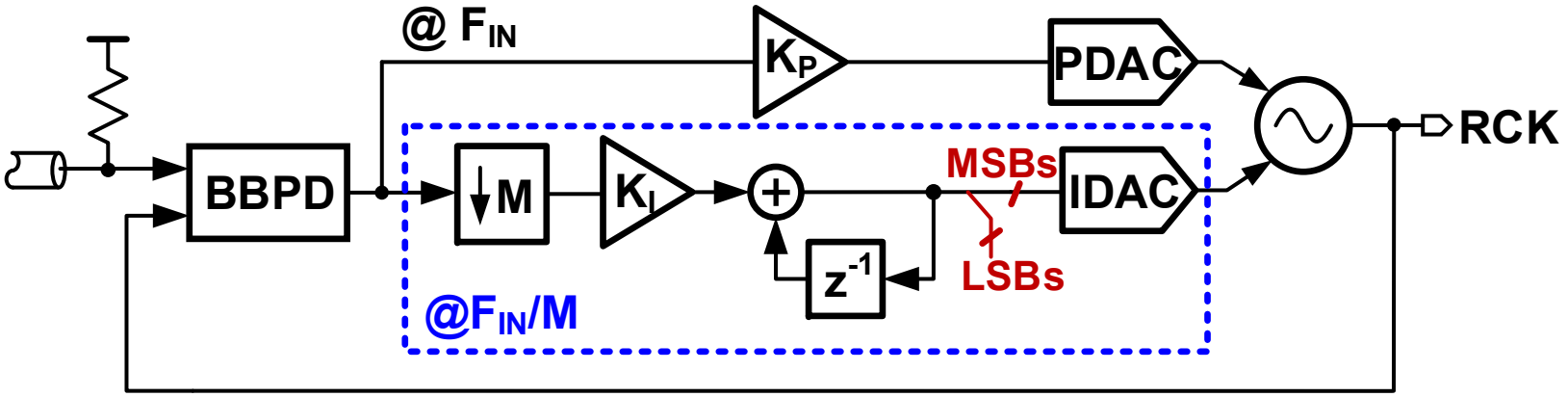


- Fast proportional path
  - Minimize latency → reduce dithering jitter

no latency

- High resolution integral path
  - Minimize tracking jitter
- Minimal hardware penalty
  - Needs only 2-level high-speed PDAC

Practical Digital CDR



- Loop delay increases integral path dithering jitter
  - Reduce gain by dropping lower LSBs
- IDAC implemented using $\Delta\Sigma$ techniques
- Proportional and integral controls summed in VCO
- Area efficient → can be fully integrated

Digital CDR Drawbacks

- Coupled JTRAN and JTOL
- Jitter peaking
- ~~Large loop filter area~~

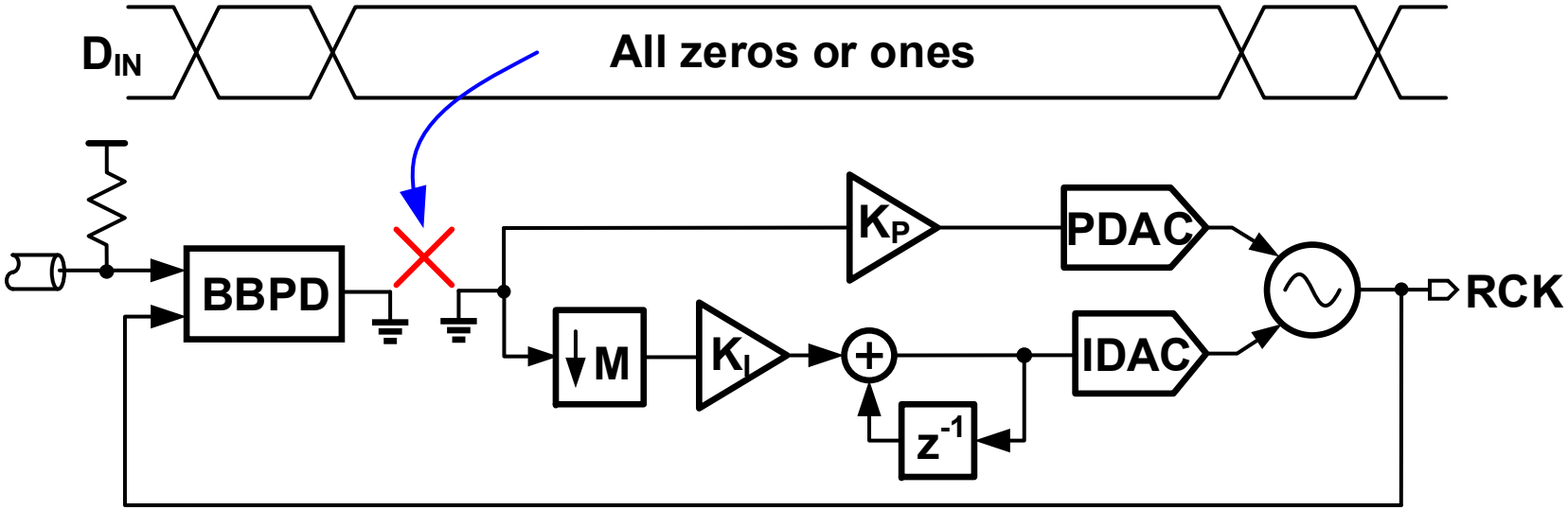
} Similar to linear CDR

- JGEN vs bang-bang step size tradeoff
- JTRAN dependence on input jitter

} Similar to BB CDR

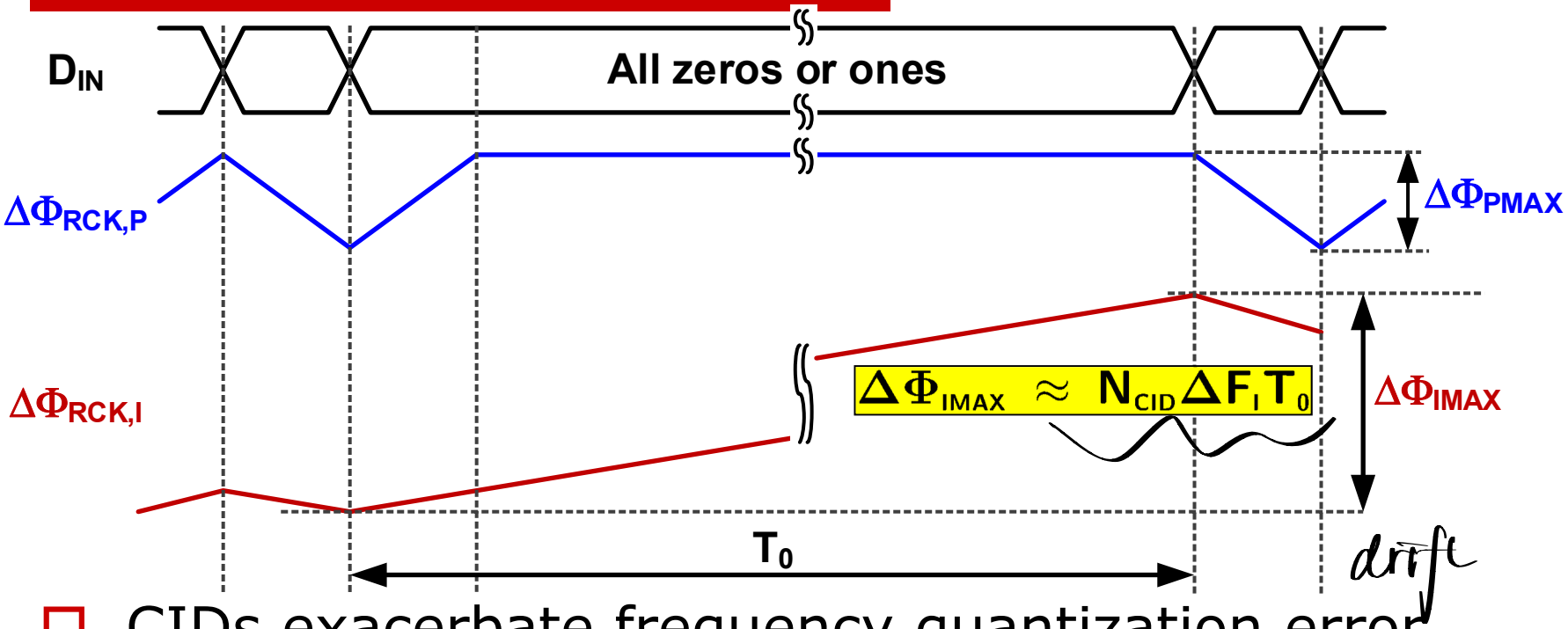
- **Sensitive to Consecutive Identical Digits (CIDs)**

Impact of CIDs[7]



- BBPD output is zero for the duration of CIDs
  - CDR operates in open loop
- All benefits of feedback are lost
  - Noise, leakage, PVT sensitivity, …

JGEN due to CIDs

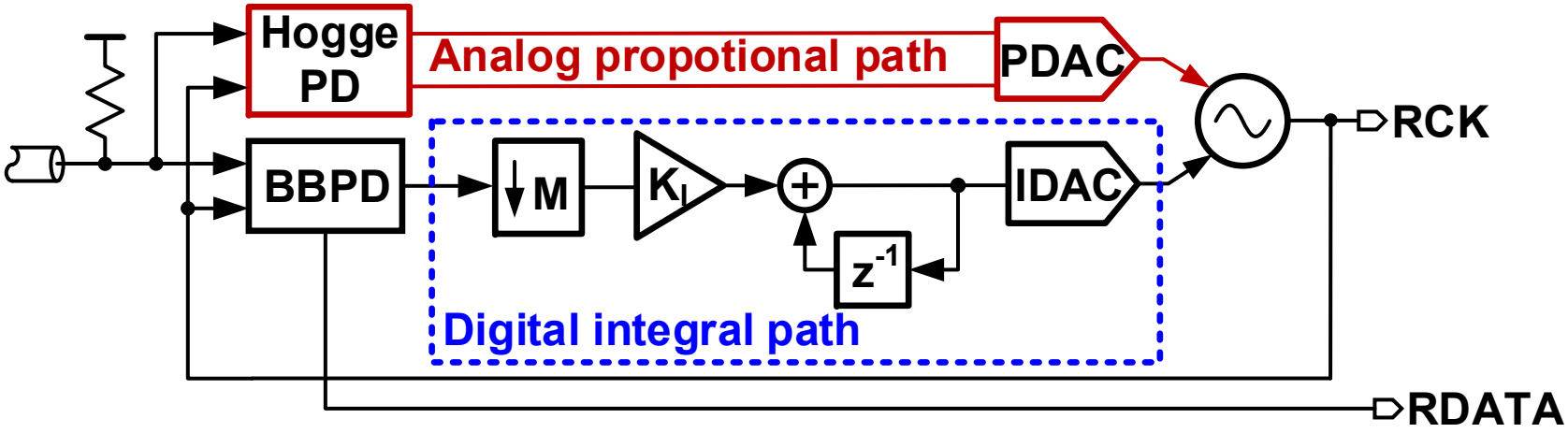


- CIDs exacerbate frequency quantization error
  - Output phase drifts at a rate proportional to freq. error
- Impact on JGEN depends on:
  - Number of CIDs (N_{CID})
  - Integral path frequency quantization error (ΔF_I)

Analog vs. Digital CDRs

- Analog CDR using linear PD
  - Well-controlled loop dynamics
  - PD non-idealities degrade timing margin/BER
  - Large loop filter capacitor
- Digital CDR using bang-bang PD
  - Non-linear loop dynamics (JTRAN depends on jitter)
  - Bang-bang PD maximizes timing margin
  - No large capacitor (small area)
- Can we combine the advantages?

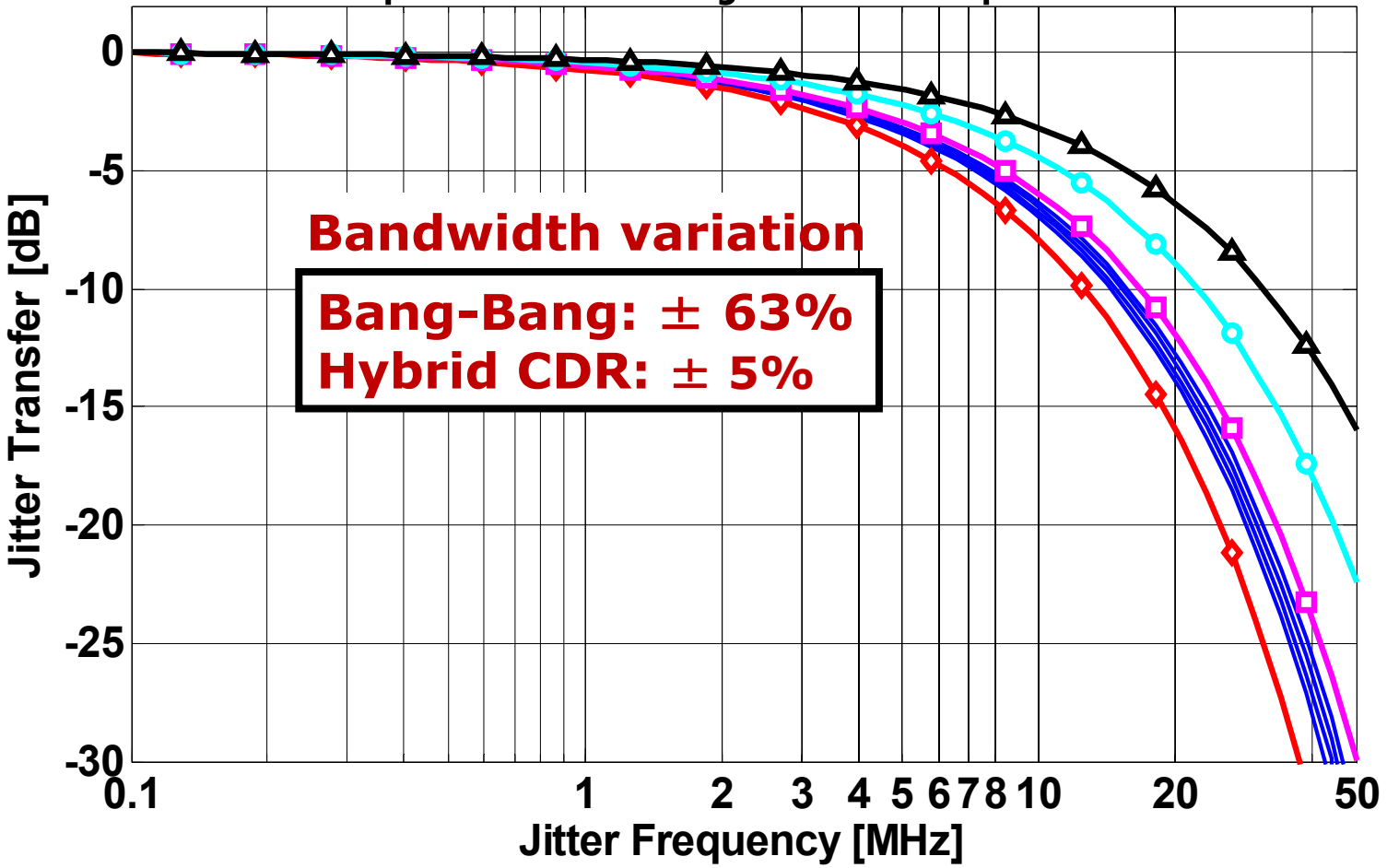
Hybrid Analog/Digital CDR[8]



- Proportional path sets loop bandwidth (JTRAN)
  - Fixed gain leads to linear loop dynamics
  - Eliminates phase quantization error
- Digital integral path sets steady state
  - Makes it insensitive to linear PD phase offset
  - Accumulator filters BBPD quantization error
  - Causes ripple on the proportional path

Hybrid CDR JTRAN Characteristics

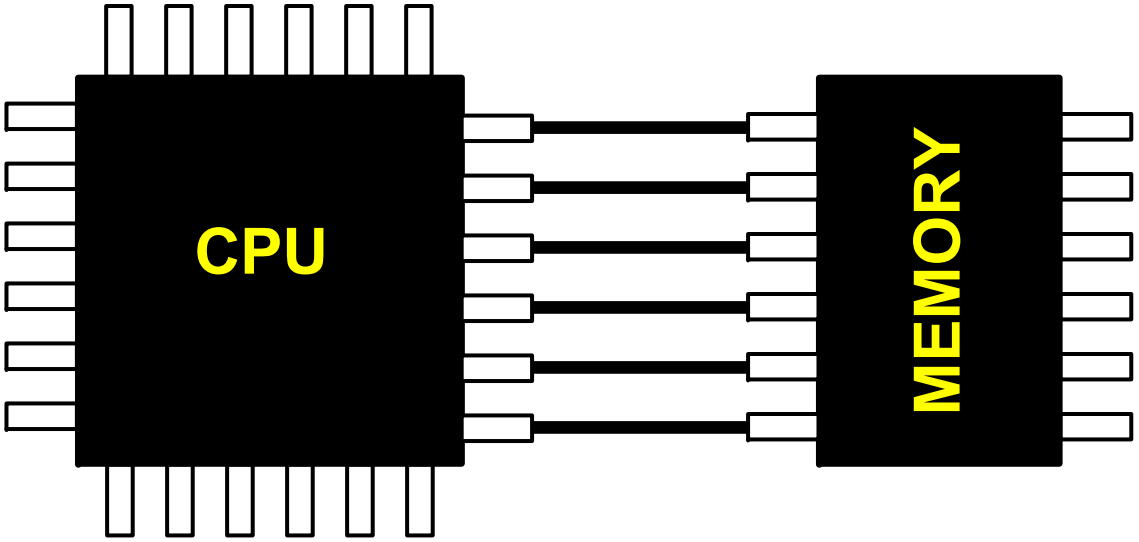
- JTRAN independent of jitter amplitude



Tutorial Roadmap

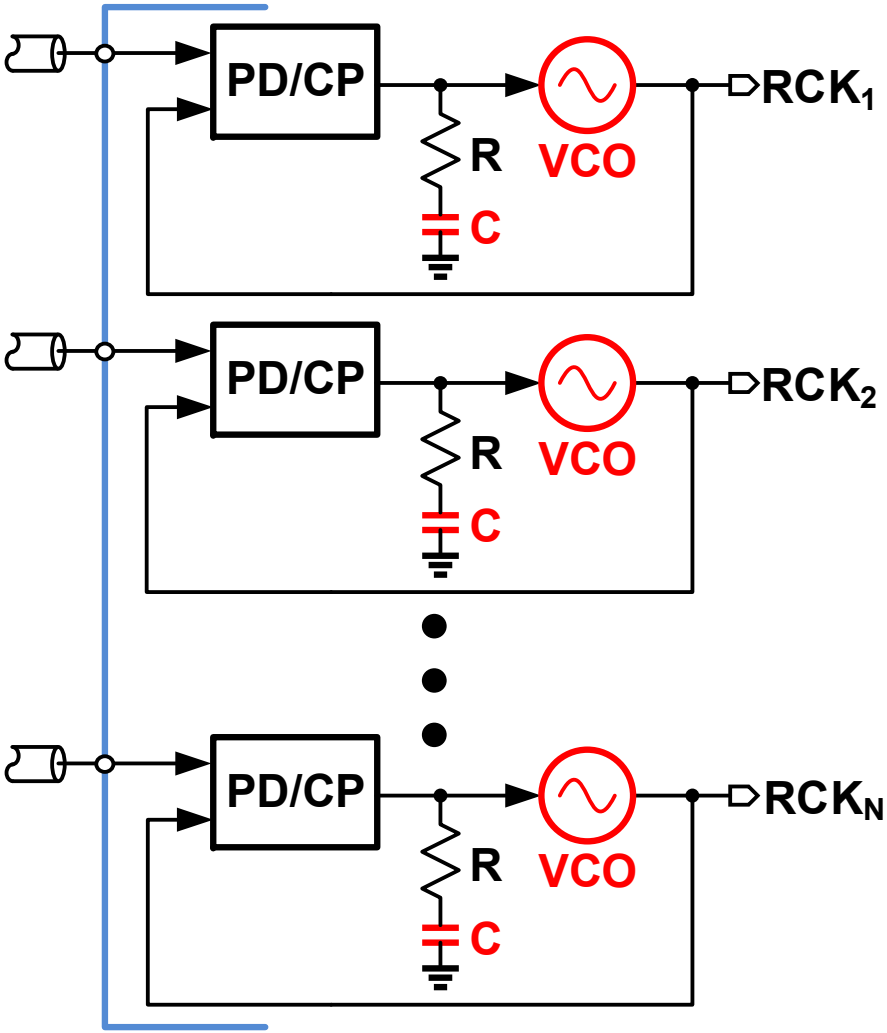
- Performance metrics
- Basic architectures
  - Linear/Bang-bang
  - Digital
  - Hybrid
- **Application-specific CDRs**
  - **Multi-lane chip-to-chip links**
  - **Repeaters for optical links and active cables**
- Summary

Multi-lane Chip-to-Chip Links



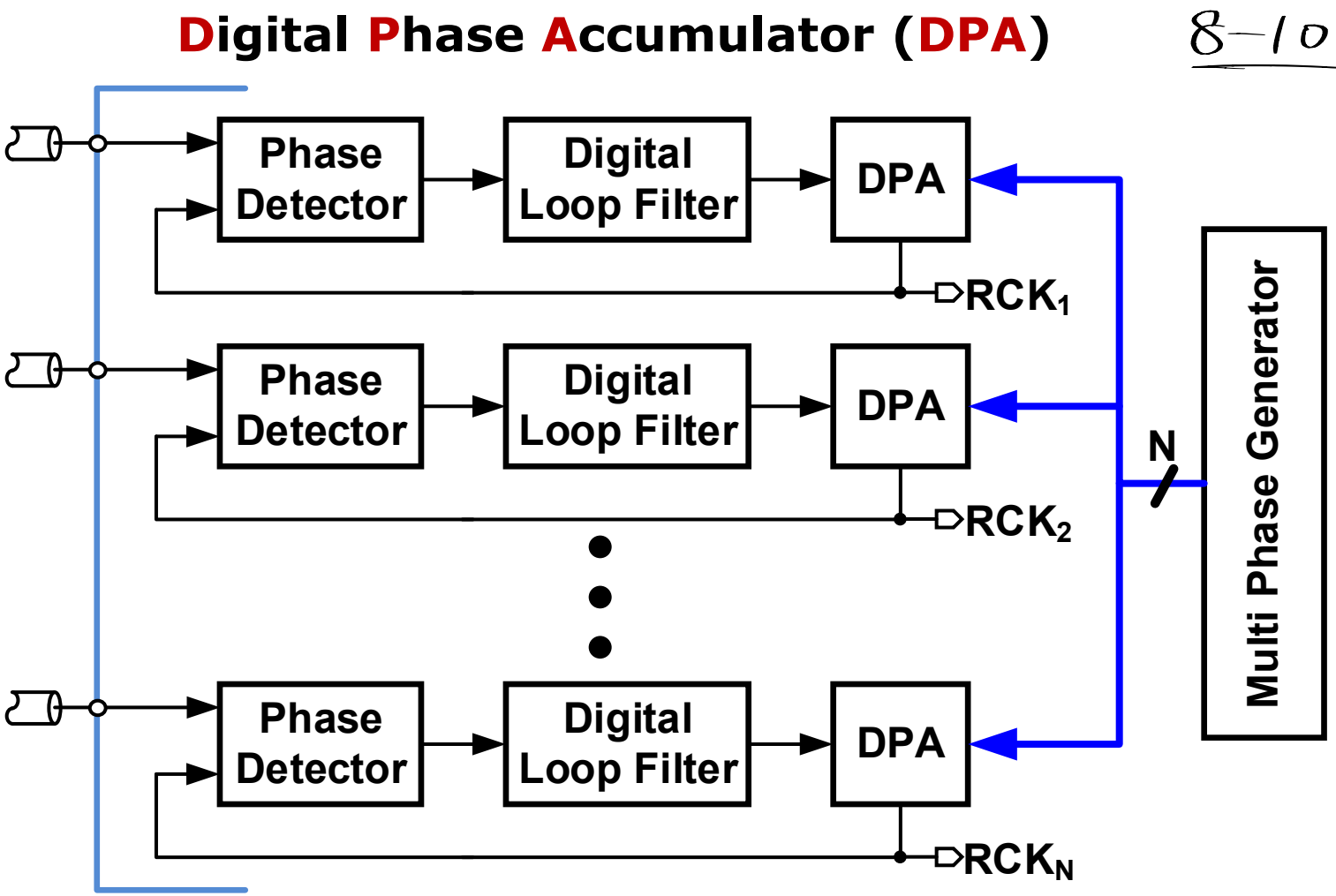
- Source synchronous clocking is common
  clock forwarding
- BUT many standards mandate embedded clocking
  - Examples: PCIe, XAUI, SATA, etc.

Multi-Lane CDR Challenges

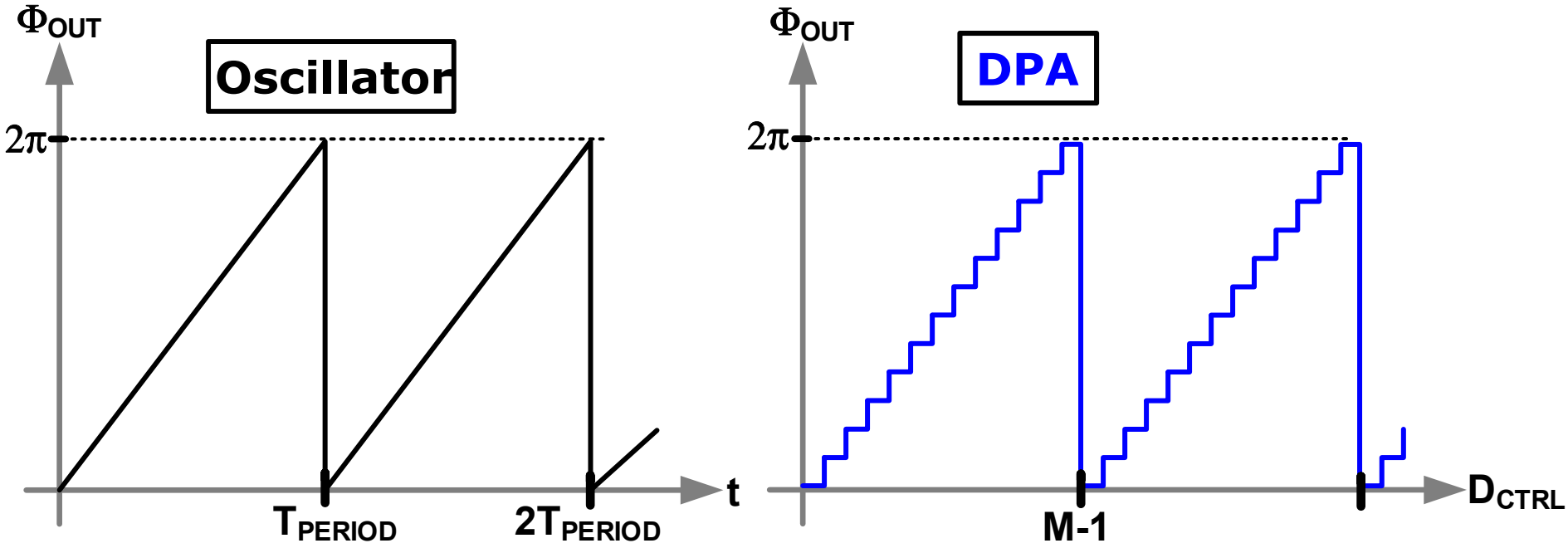


- Many VCOs & capacitors
- Large area
- Harmonic locking

Multi-Lane CDR Solution

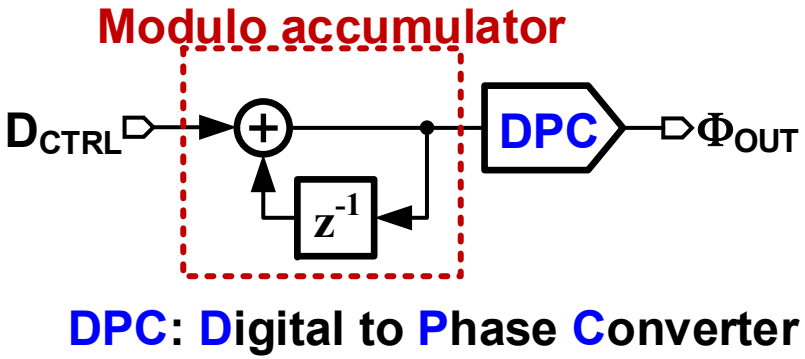


Digital Phase Accumulator (DPA)



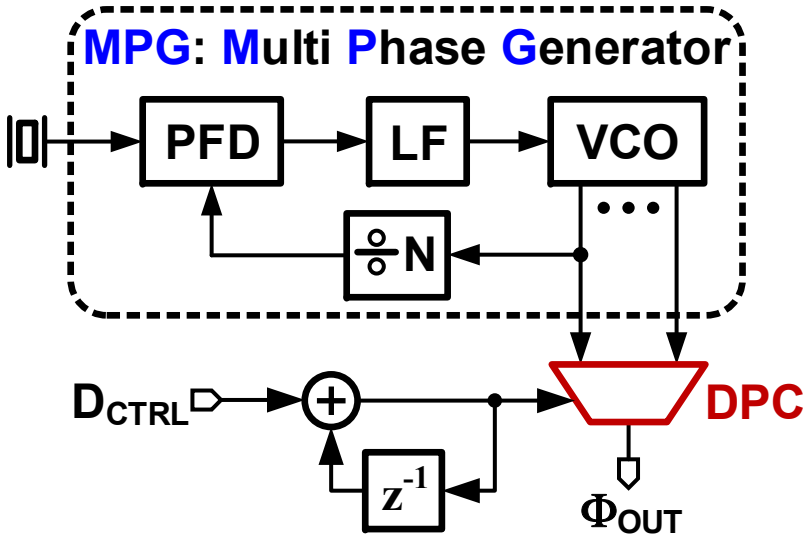
- Oscillators are phase accumulators
  - Modulo 2π accumulation
- Mimic oscillator operation
  - Explicit phase accumulation
  - Infinite phase shifting by modulo accumulation

Conceptual DPA Realization



- Digital accumulator mimics phase accumulation
  - Rate governed by clock frequency
  - Modulo arithmetic maps 2π phase to 0
- DPC generates output phase
  - DPC non-idealities directly appear at the output

Practical DPA Realization

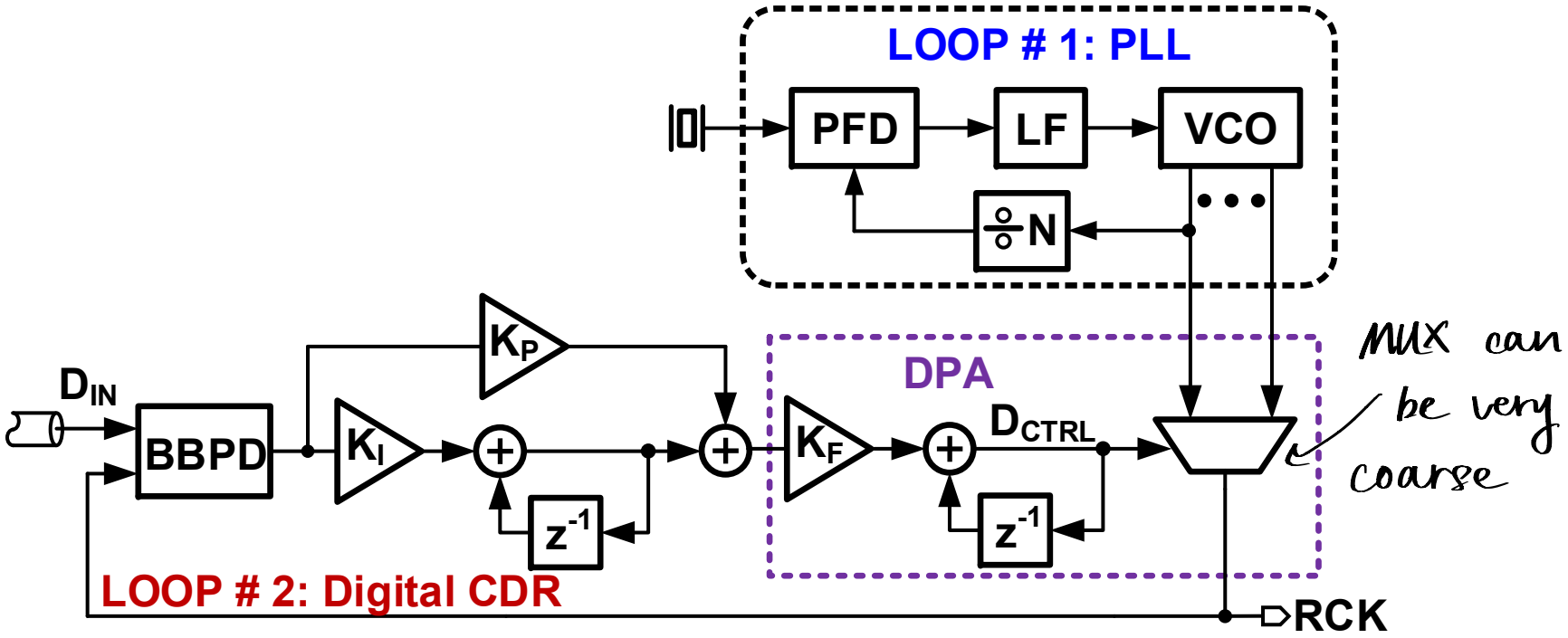


- DPC implemented using a mux

$$\Phi_{OUT} = \Phi_{VCO} + D_{CTRL} \cdot K_{DPC}$$

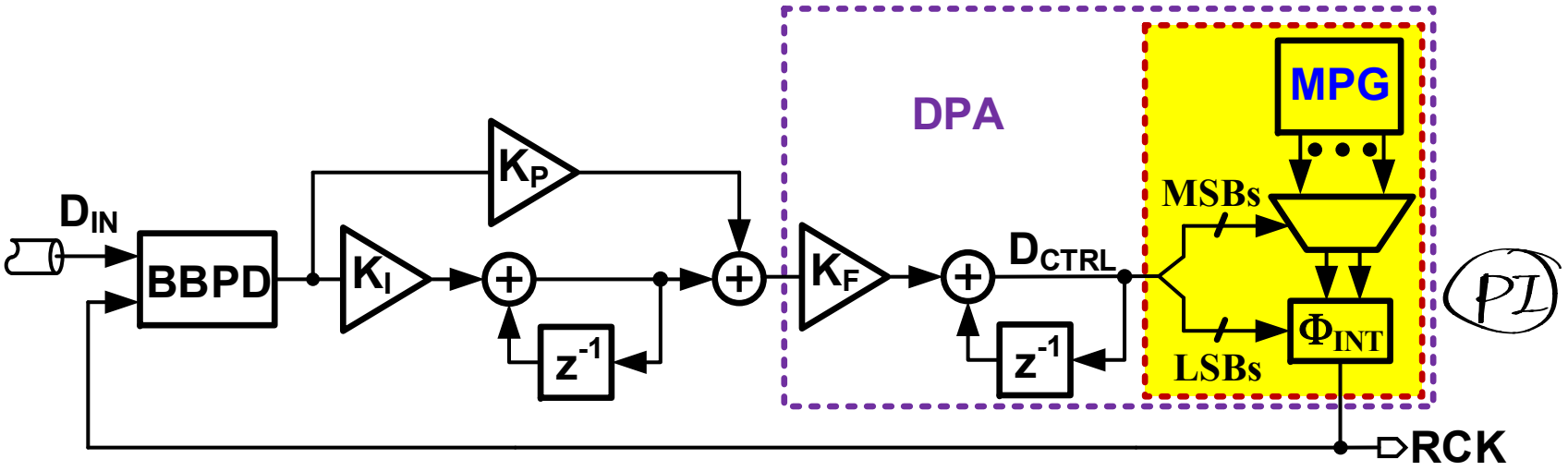
$$\text{For M-phase VCO}: \; K_{DPC} = \frac{2\pi}{M}$$

Dual-Loop CDR[9]



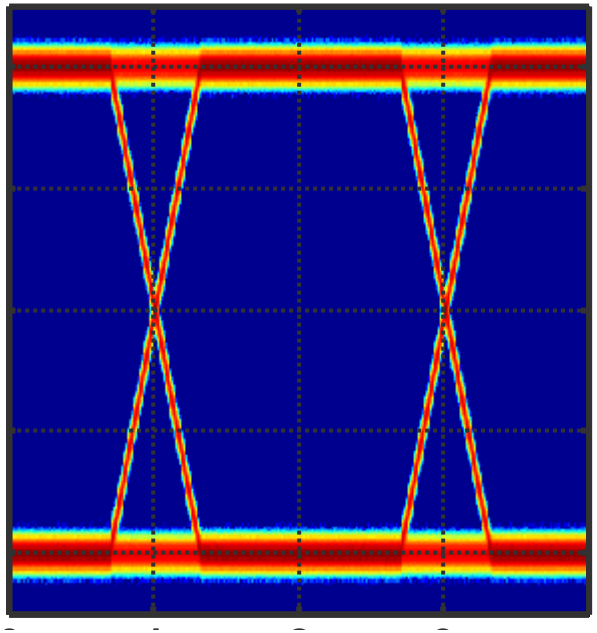
- Dual loop: Loop # 1: PLL(MPG), Loop # 2: CDR
- DPA replaces DCO in the CDR
- PLL guarantees frequency locking

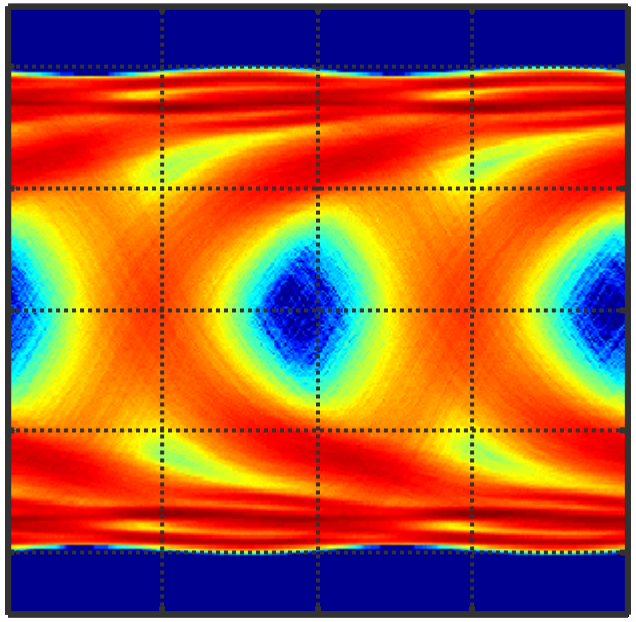
Practical Dual-Loop CDR[10]



- Phase interpolator (Φ_{INT}) improves DPA resolution
  - Better JGEN
- PI resolution depends on many factors
  - Input rise time, input phase spacing, PI BW,…

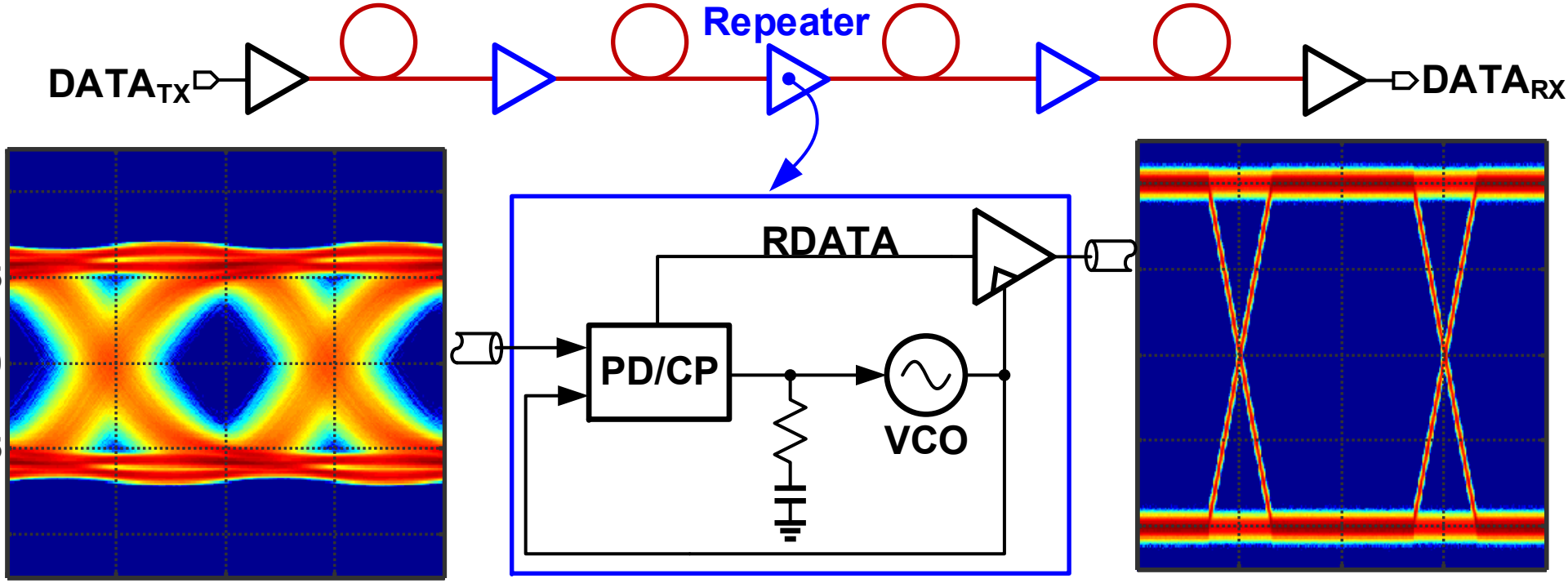
Long-Haul Communication





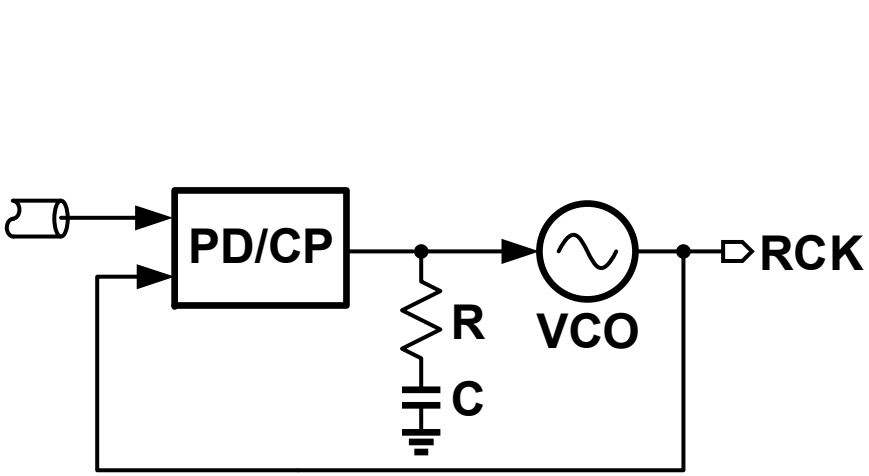
- Difficult to achieve error-free operation

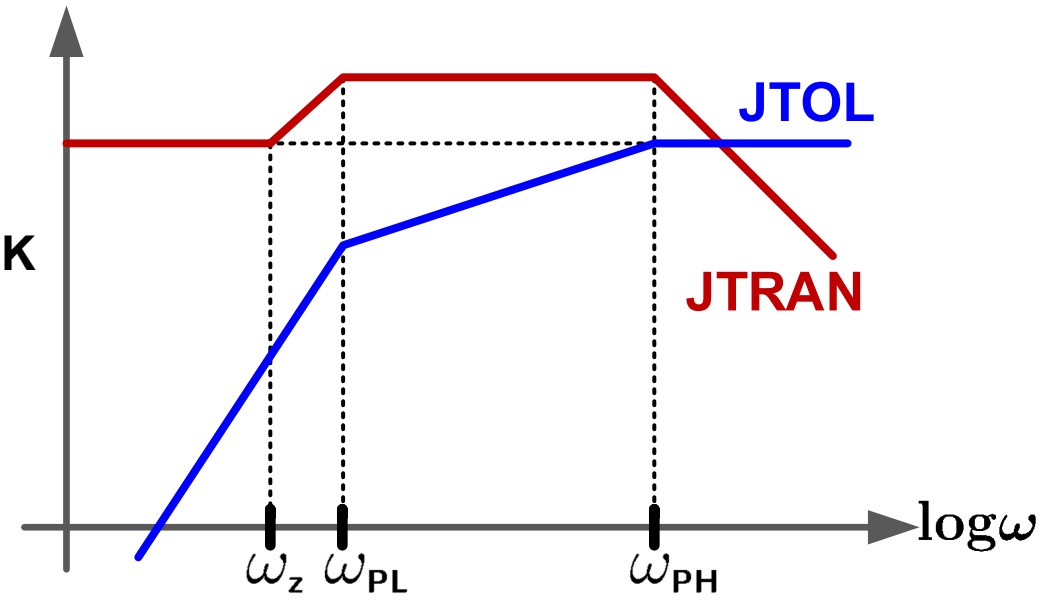
Active Repeaters



- Repeater requirements
  - Tolerate large input jitter (high JTOL)
  - Filter input jitter (low JTRAN) w/ minimal peaking
  - Re-transmit with low jitter (Low JGEN)

How About Conventional CDR?





- Jitter peaking → large loop filter capacitor

small jitter peaking.

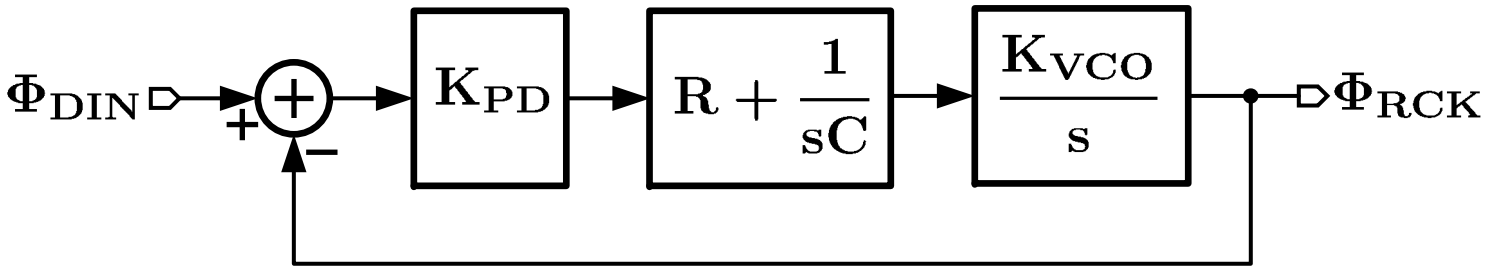
- High JTOL → high JTRAN

due to coupling

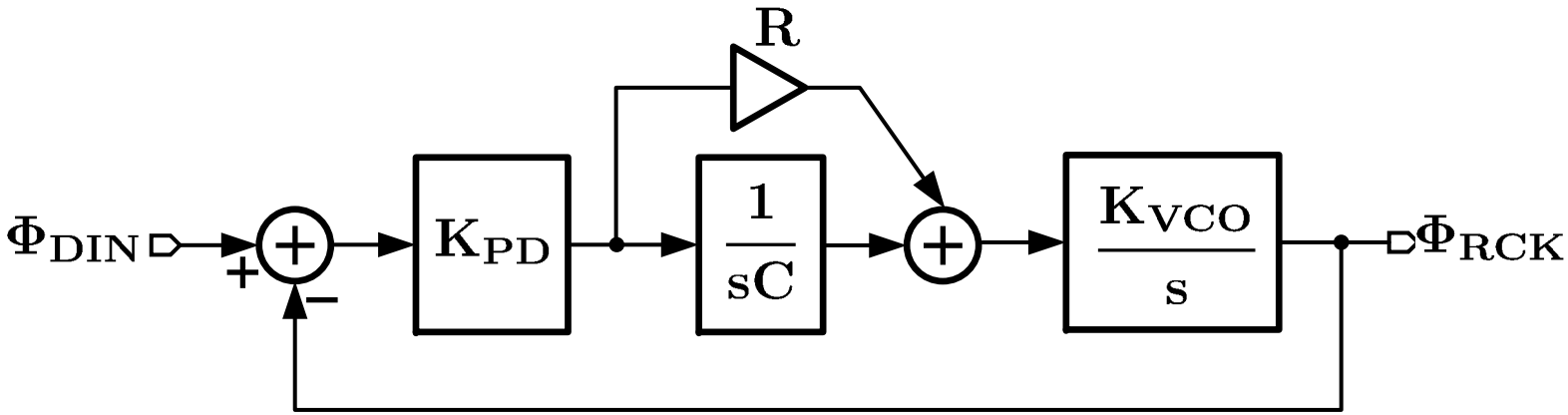
  - Cannot adequately filter i/p jitter → degrades RCK jitter

How to Eliminate Jitter Peaking?

- **Main idea:** Remove zero in feed-forward path

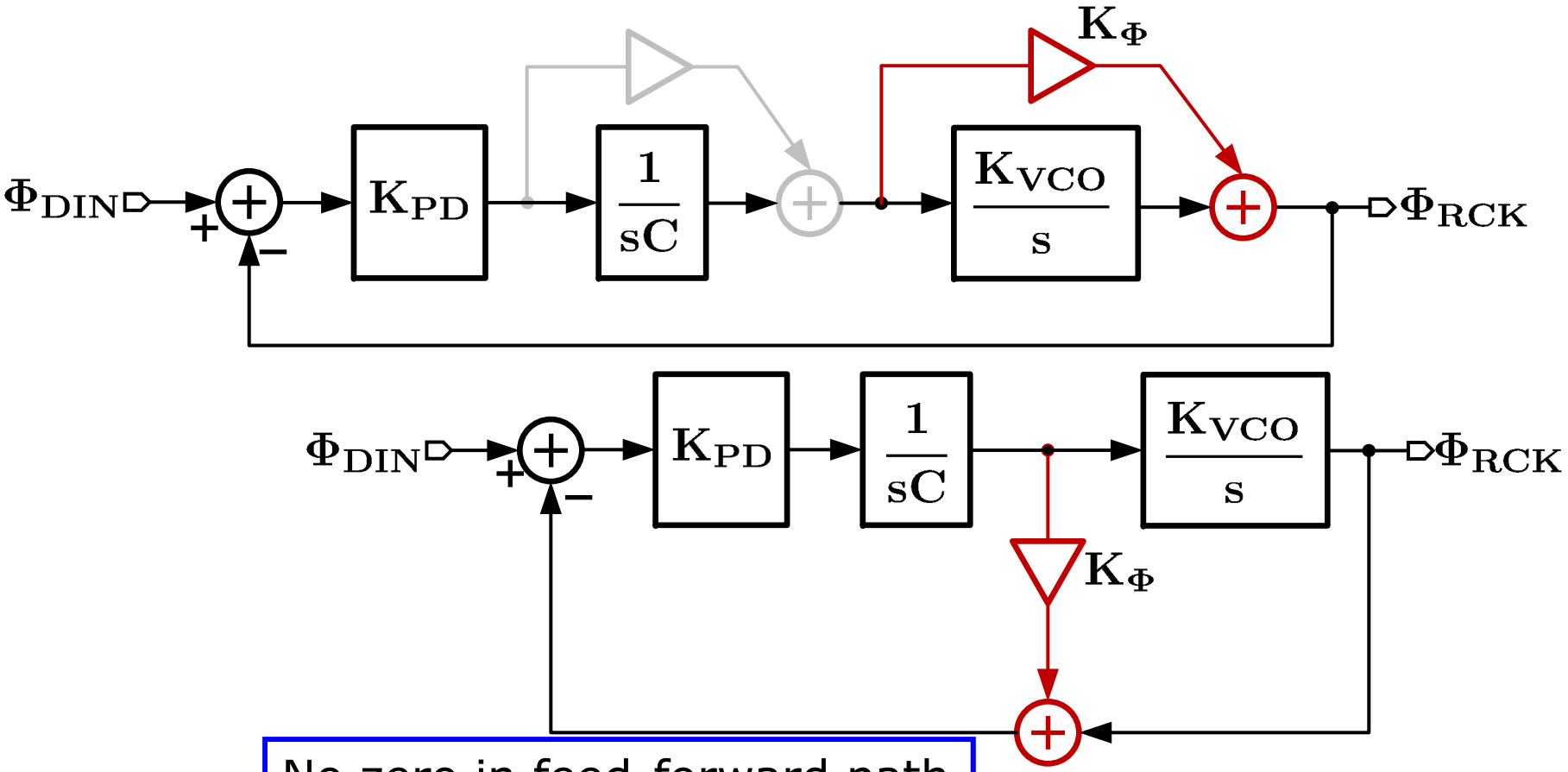


Feed-forward across **current** integrator



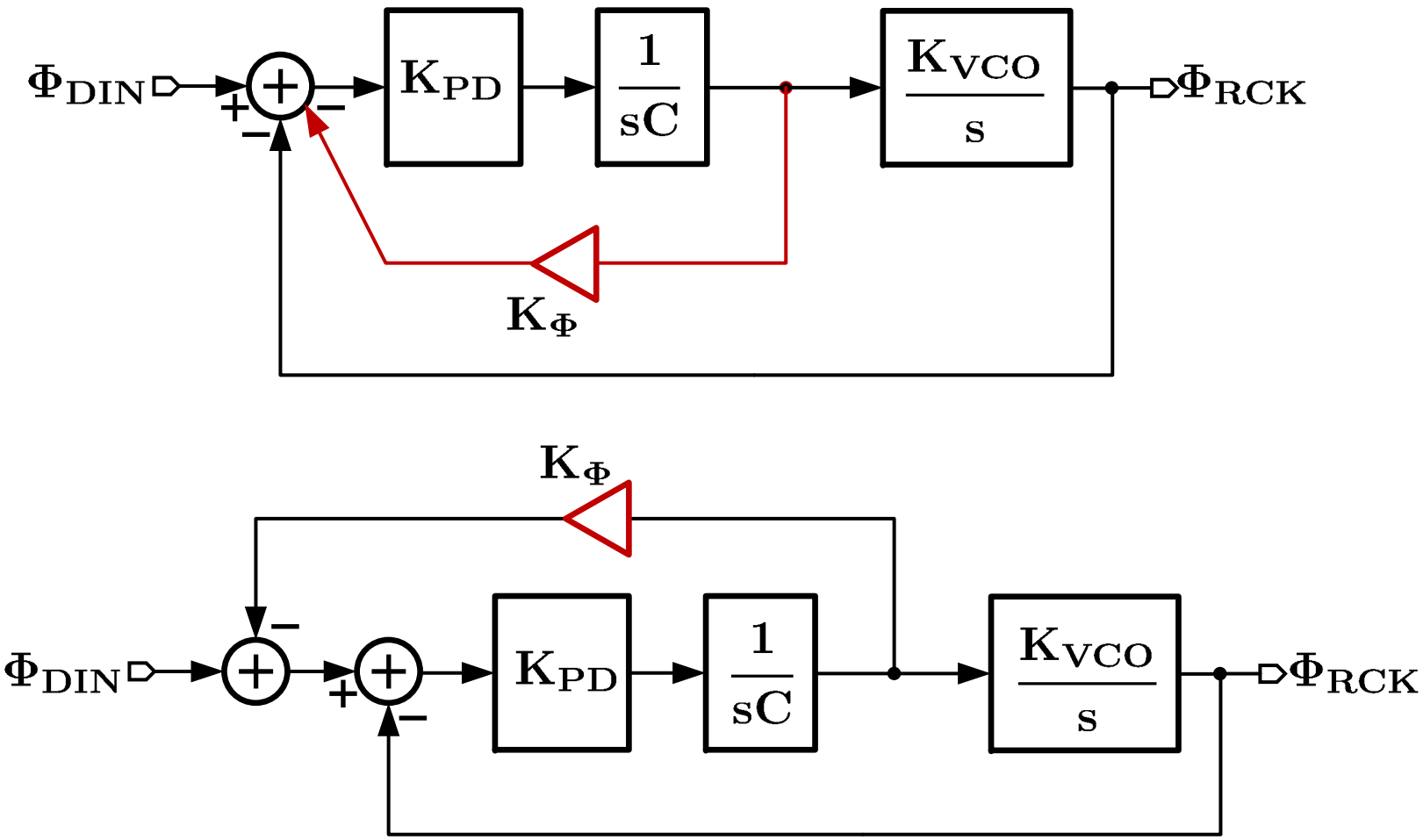
Eliminate Jitter Peaking (I)[11]

Feed-forward across **phase** integrator (VCO)

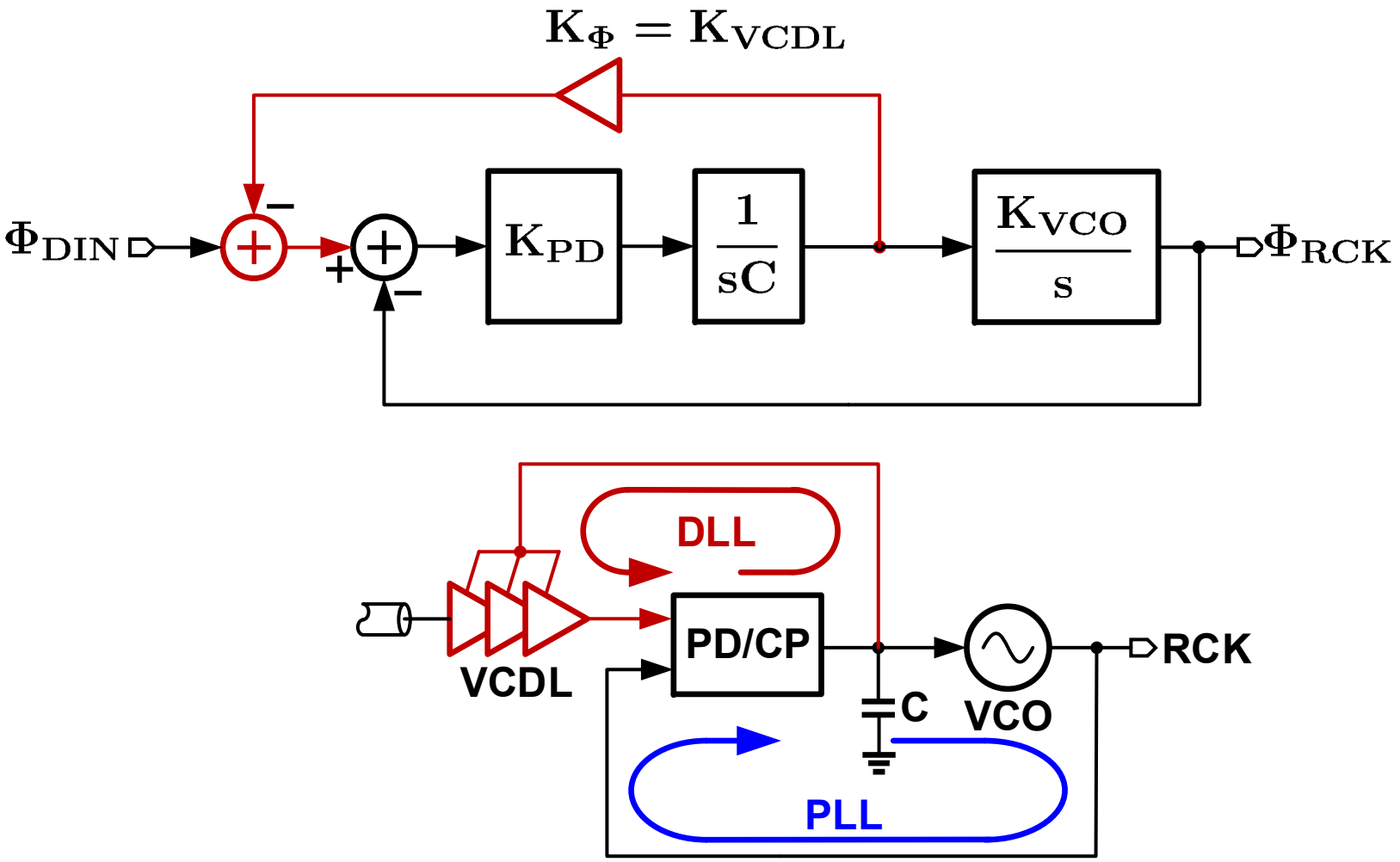


No zero in feed-forward path

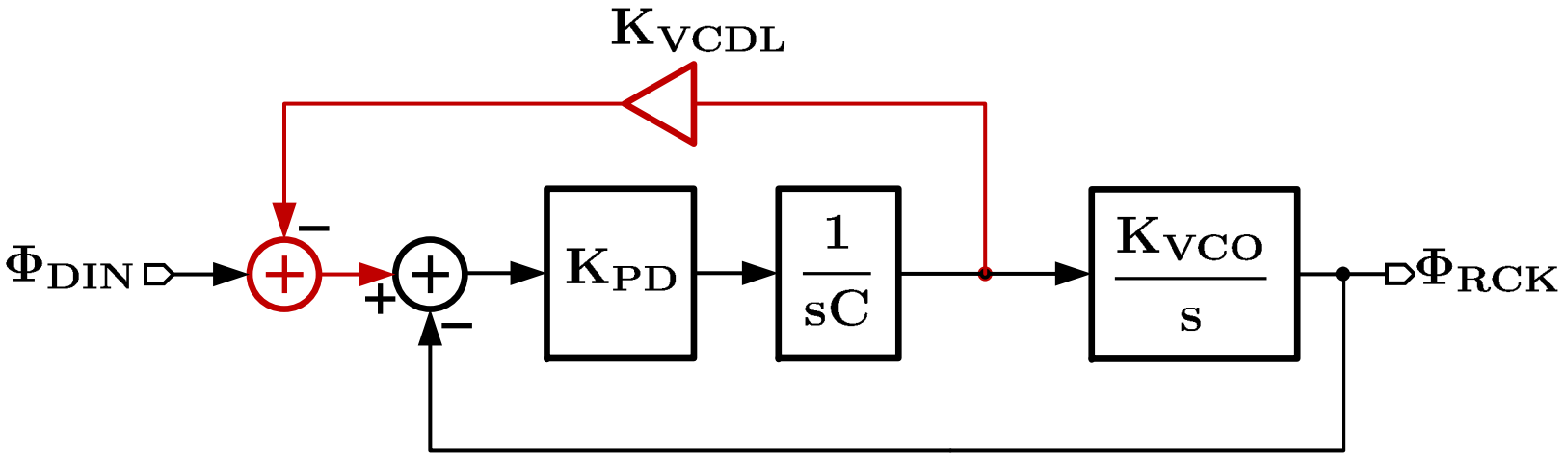
Eliminate Jitter Peaking (II)



CDR w/ No Jitter Peaking



D/PLL CDR Jitter Transfer (I)



$$LG_{PLL}(s) = K_{PD} \cdot \frac{1}{sC} \cdot \frac{K_{VCO}}{s}; \quad LG_{DLL}(s) = K_{PD} \cdot \frac{1}{sC} \cdot K_{VCDL}$$

$$H_{JTRAN}(s) = \frac{\Phi_{RCK}(s)}{\Phi_{DIN}(s)} = \frac{LG_{PLL}(s)}{1 + LG_{PLL}(s) + LG_{DLL}(s)}$$

$$= \frac{1}{1 + s \cdot \frac{K_{VCDL}}{K_{VCO}} + s^2 \cdot \frac{C}{K_{VCO} K_{PD}}}$$

no zero, no peaking if overdamped.

D/PLL CDR Jitter Transfer (II)

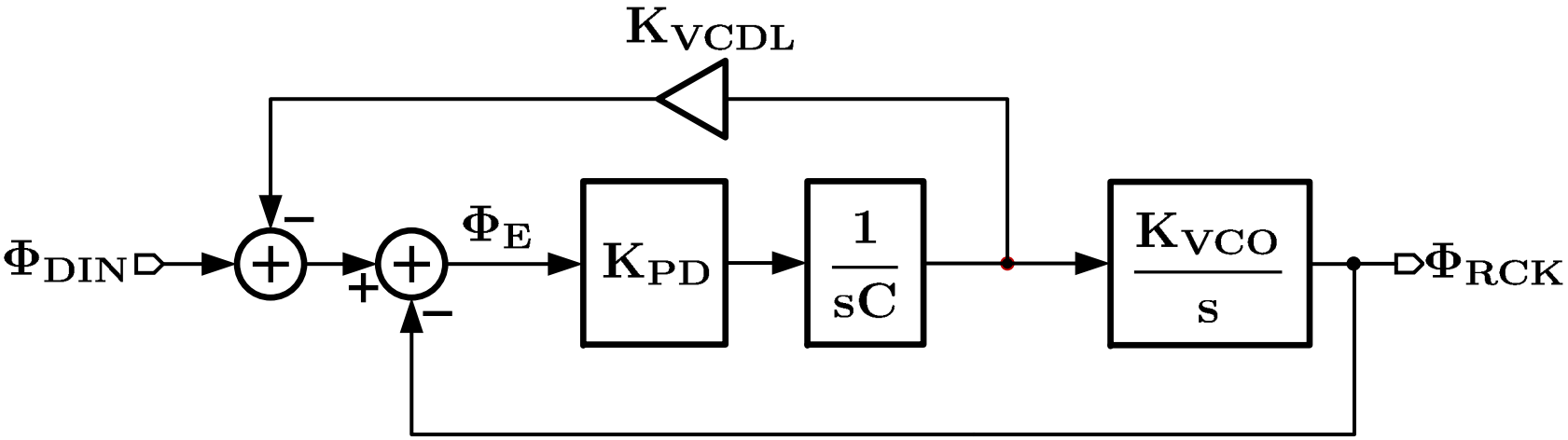
$$H_{JTRAN}(s) = \frac{1}{1 + s \cdot \frac{K_{VCDL}}{K_{VCO}} + s^2 \cdot \frac{C}{K_{VCO} K_{PD}}} \equiv \frac{1}{(1 + s/\omega_{PL})(1 + s/\omega_{PH})}$$

$$\Longrightarrow \quad \omega_{PL} \approx K_{VCO}/K_{VCDL};\ \omega_{PH} \approx K_{VCDL} \cdot K_{PD}/C$$

$$\text{JTRAN BW} = \omega_{-3dB} \approx \omega_{PL} = K_{VCO}/K_{VCDL}$$

- No jitter peaking if damping factor > 0.707
- JTRAN BW = lower of the 2 pole frequencies

D/PLL CDR Jitter Tolerance (I)



$$H_{JTRACK}(s) = \frac{\Phi_E(s)}{\Phi_{DIN}(s)} = \frac{1}{1 + LG_1(s) + LG_2(s)}$$

$$= \frac{s^2 \cdot \frac{C}{K_{VCO}K_{PD}}}{1 + s \cdot \frac{K_{VCDL}}{K_{VCO}} + s^2 \cdot \frac{C}{K_{VCO}K_{PD}}}$$

$$\equiv \frac{s^2/\omega_{PL}\omega_{PH}}{(1 + s/\omega_{PL})(1 + s/\omega_{PH})}$$

D/PLL CDR Jitter Tolerance (II)

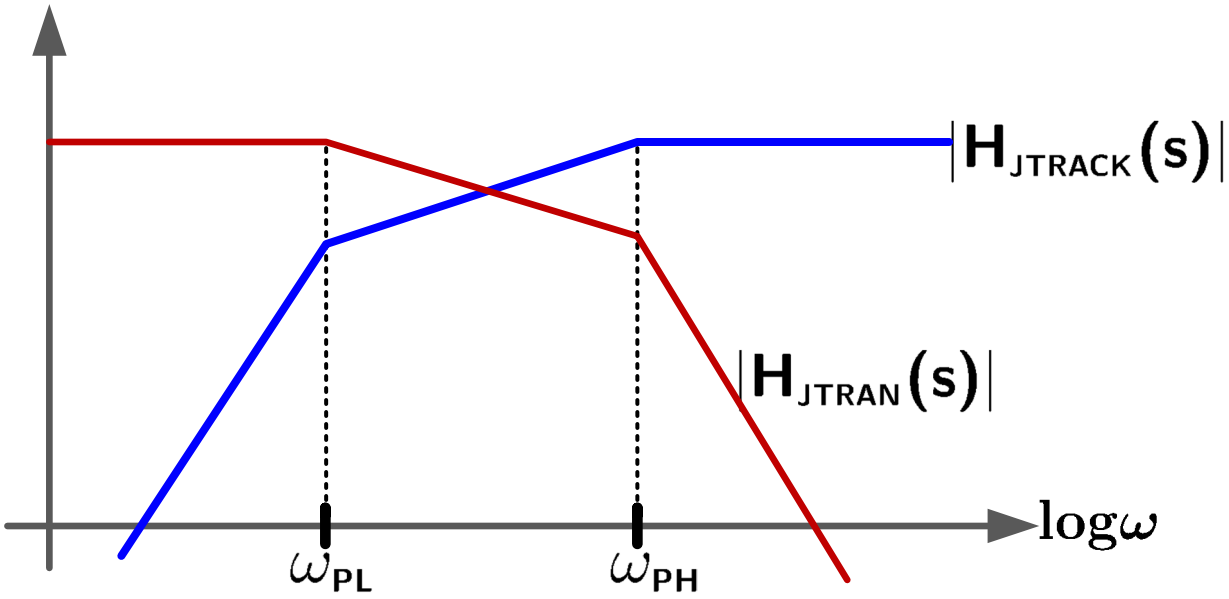
$$H_{JTRACK}(s) = \frac{s^2 \cdot \frac{C}{K_{VCO}K_{PD}}}{1 + s \cdot \frac{K_{VCDL}}{K_{VCO}} + s^2 \cdot \frac{C}{K_{VCO}K_{PD}}} \equiv \frac{s^2/\omega_{PL}\omega_{PH}}{(1 + s/\omega_{PL})(1 + s/\omega_{PH})}$$

$$\Longrightarrow \quad \omega_{PL} \approx K_{VCO}/K_{VCDL};\ \omega_{PH} \approx K_{VCDL} \cdot K_{PD}/C$$

JTRACK/JTOL Corner $= \omega_{-3dB} \approx \omega_{PH} \approx K_{VCDL} \cdot K_{PD}/C$

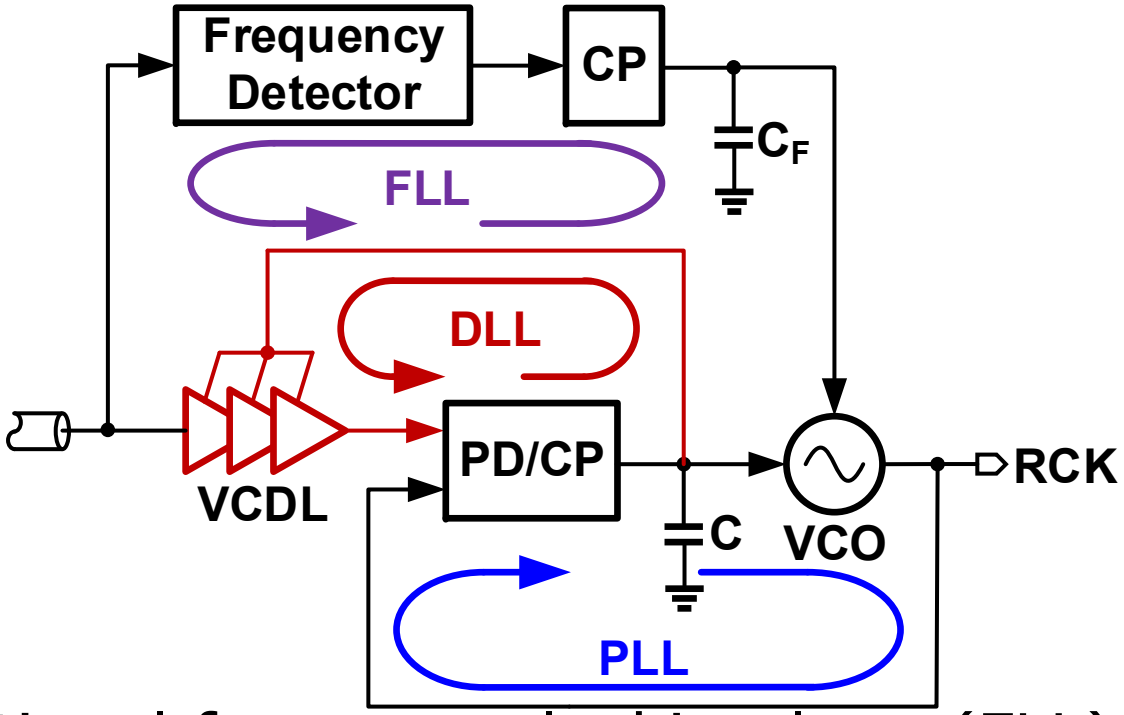
- JTOL corner = higher of the 2 pole frequencies

D/PLL CDR JTRAN vs. JTOL



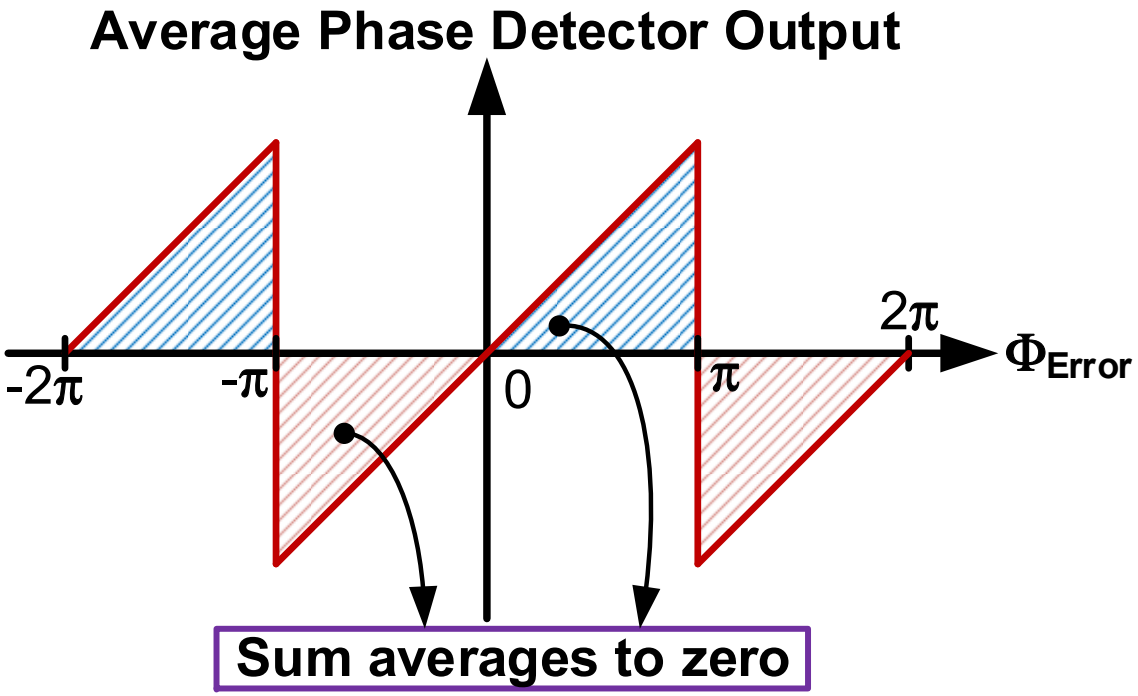
- **Decoupled** JTRAN and JTOL
  - ω_{PL} sets JTRAN BW
  - ω_{PH} sets JTOL corner frequency

A Practical D/PLL CDR



- Additional frequency-locking loop (FLL)
- Challenges:
  - Frequency detection of random data
  - Interaction between FLL and PLL

Limited Capture Range

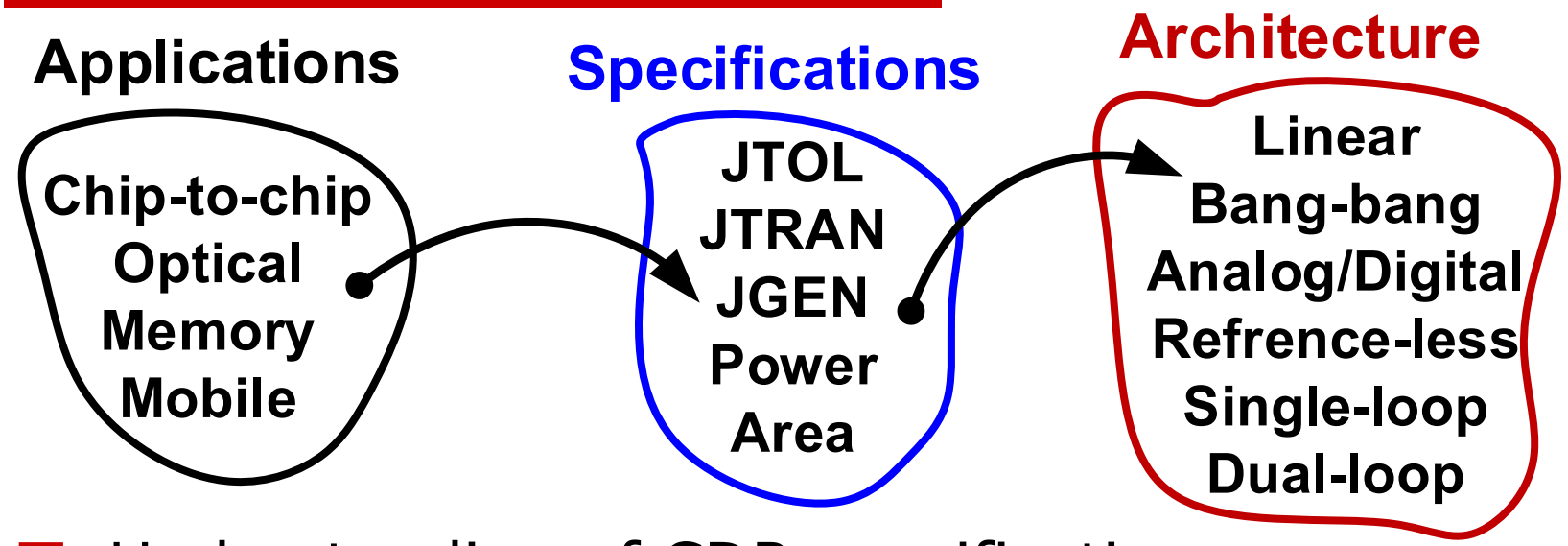


- Symmetric PD transfer characteristic
- Avg. PD output becomes zero w/ frequency error
  - PD cannot detect large frequency error

Frequency Detectors

- Rotational frequency detector[12-14]
- Quadri-correlator frequency detector[15-16]
- Stochastic reference clock generator[17]
- Miscellaneous FDs
  - Strobed linear PD[18]
  - Counting BBPD outputs [19]

Summary



- Understanding of CDR specifications
  - What are the important jitter metrics for a given app.?
- Understanding of CDR architectures
  - What is the best architecture for a given app.?
- CDR design techniques
  - How to choose the loop parameters?

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Related ISSCC 2015 Papers

- Papers 22.7 & 22.8: Reference-less CDRs for beyond 25Gb/s optical links
- 22.1 & 3.7: Fast locking CDR for burst-mode applications
- 3.1: Quarter-rate dual loop CDR
- 10.5: Baud-rate CDR

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